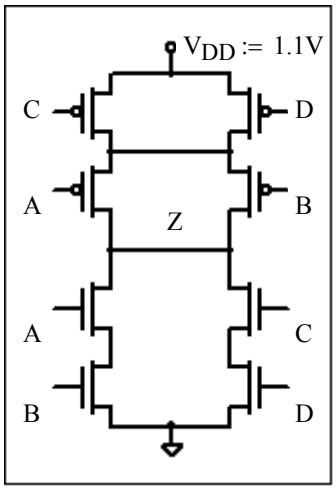
NTU 6342 / EE 241 Homework #2
Solutions

Problem 1:

For the CMOS implementation:



$$Z = \overline{(A \cdot B + C \cdot D)}$$

Simulation results (ABCD: 1000 -> 0111):

$t_{pLH} := 45.111ps \qquad E_{LH} := 8.3245fJ$

$EDP_{LH} := t_{pLH} \cdot E_{LH} \qquad EDP_{LH} = 375.527\ ps \cdot fJ$

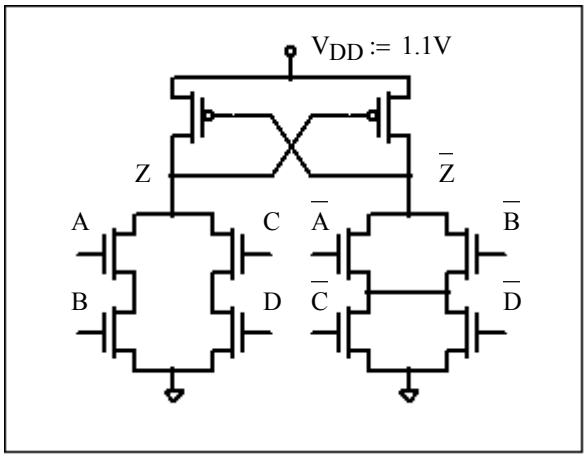
Simulation results (ABCD: 1111 -> 1010):

$t_{pHL} := 33.006ps \qquad E_{HL} := 16.813fJ$

$EDP_{HL} := t_{pHL} \cdot E_{HL} \qquad EDP_{HL} = 554.93\ ps \cdot fJ$

$$t_p := \frac{t_{pHL} + t_{pLH}}{2} \qquad t_p = 39.059\ ps$$

For the DCVSL implementation:

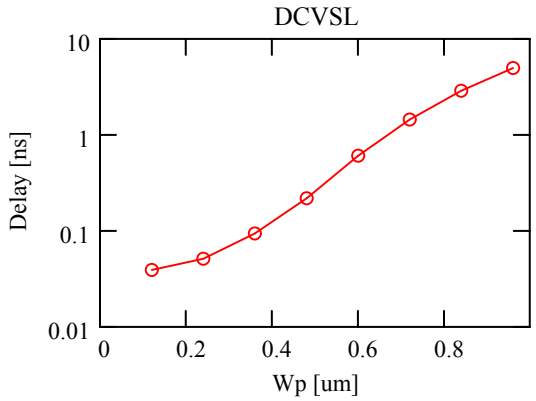


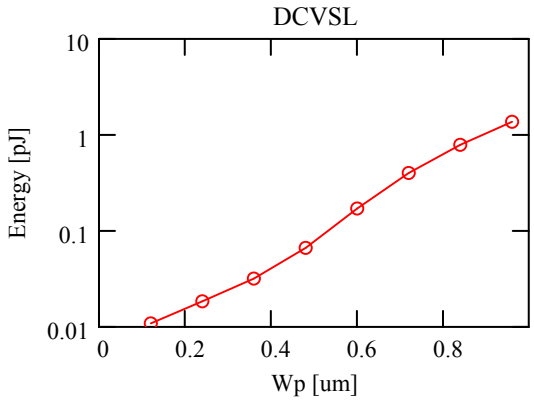
$$Z = \overline{(A \cdot B + C \cdot D)}$$

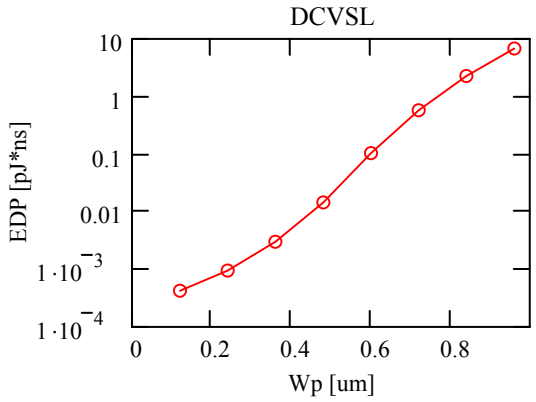
$$W_p := \begin{pmatrix} 0.12\mu m \\ 0.24\mu m \\ 0.36\mu m \\ 0.48\mu m \\ 0.60\mu m \\ 0.72\mu m \\ 0.84\mu m \\ 0.96\mu m \end{pmatrix}$$

$$t_p := \begin{pmatrix} 38.922\,ps \\ 51.026\,ps \\ 93.912\,ps \\ 0.21786\,ns \\ 0.60354\,ns \\ 1.4437\,ns \\ 2.8657\,ns \\ 4.9542\,ns \end{pmatrix} \quad E_{ave} := \begin{pmatrix} 10.869\,fJ \\ 18.393\,fJ \\ 31.773\,fJ \\ 66.280\,fJ \\ 0.17078\,pJ \\ 0.39834\,pJ \\ 0.78823\,pJ \\ 1.3683\,pJ \end{pmatrix}$$

$$EDP := \overrightarrow{(t_p \cdot E_{ave})} \qquad EDP = \begin{pmatrix} 0.423 \\ 0.939 \\ 2.984 \\ 14.44 \\ 103.073 \\ 575.083 \\ 2.259 \times 10^3 \\ 6.779 \times 10^3 \end{pmatrix} fJ \cdot ns$$

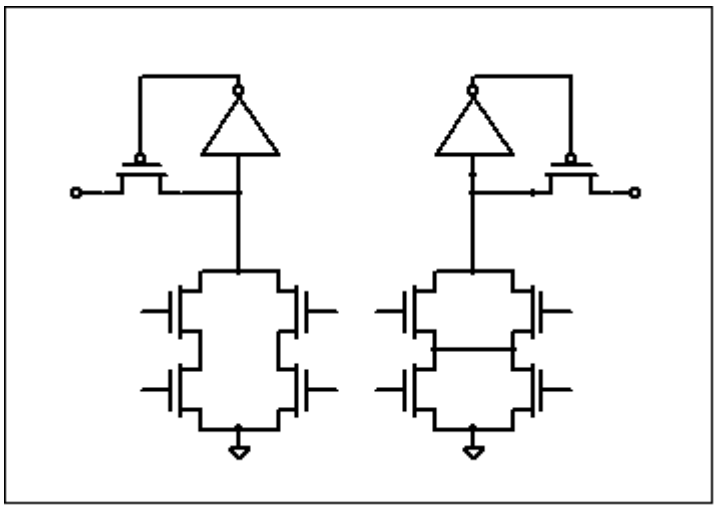






Minimum width is optimal.

Modified DCVSL Implementation:



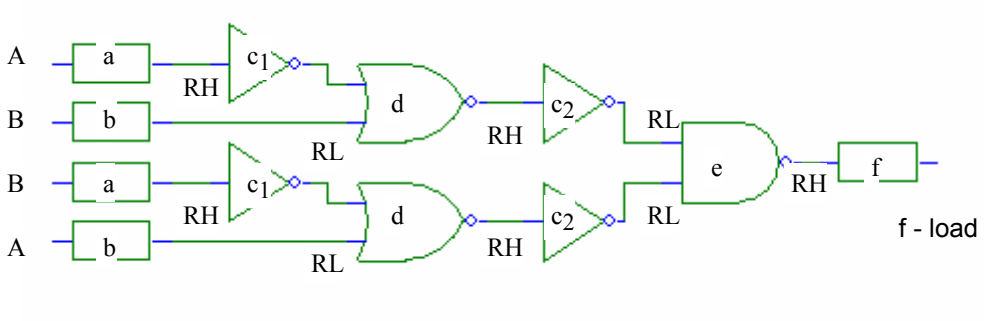
For small sizes of the PMOS keepers, the output nodes before the inverters will not be able to reach logic '1'. However, if the leakage of the PMOS keepers are large enough, then the leakage current may be able to charge up these nodes.

Problem #2:

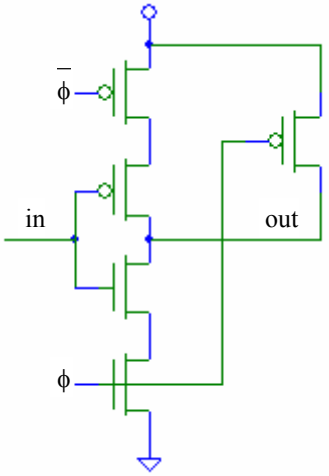
Part a:

Pulse Static CMOS XOR Gate

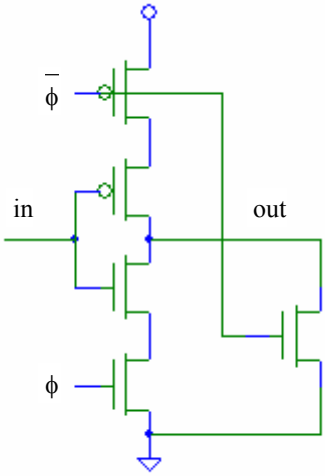
$$A \oplus B = \overline{A} \cdot B + \overline{B} \cdot A = \overline{\left(\overline{\left(A \cdot \overline{B}\right)} \cdot \overline{\left(\overline{A} \cdot B\right)}\right)} = \overline{\left[\left(\overline{A} + B\right) \cdot \left(A + \overline{B}\right)\right]}$$



a - clocked inverter with reset high



b - clocked inverter with reset low



Part b:

Optimize each gate for the required transition:

Inverter c: optimize for low to high transition

$W_n = \frac{W_p}{4}$ $\quad g_c := \frac{5}{6}$

NOR d: optimize for high to low transition

$W_n = W_p$ $\quad g_d := \frac{2}{3}$

NAND e: optimize for high to low transition

$W_n = 2 \cdot W_p$ $\quad g_e := 1$

$G := g_c \cdot g_d \cdot g_c \cdot g_e$ $\quad G = 0.463$

Assume that the XOR gate drives a fanout of 4 inverters with the same size as c1:

$F := 4$ $\quad N := 4$

$H := G \cdot F$ $\quad H = 1.852$ $\quad h := \sqrt[N]{H}$ $\quad h = 1.167$

Assume c1 is unit sized: $\quad c_1 := 1$

$d := \frac{h}{g_d \cdot g_c}$ $\quad d = 2.1$ $\quad c_2 := \frac{h}{g_c} \cdot d$ $\quad c_2 = 2.939$

$e := \frac{h}{g_e} \cdot c_2$ $\quad e = 3.429$ $\quad load := h \cdot e$ $\quad load = 4$

Sizes:

$c_1 = 1$ $\quad d = 2.1$ $\quad c_2 = 2.939$ $\quad e = 3.429$

Note that due to the limitation of the pulsed static CMOS logic family's ability to optimize only successive NAND-NOR chains, effectively one big AND function, the last gate NAND(e) is being optimized for the wrong transition (high-to-low instead of low-to-high, where the parallel transistors are).

This is due to the fact that the XOR function cannot be decomposed into purely AND components.

Problem #3:

$V_{th} := 300mV$

Part a:

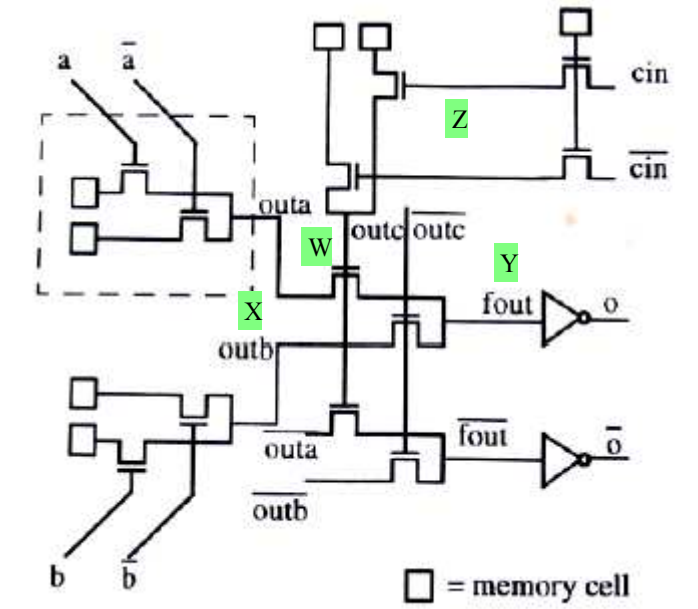
If we assume that the switching threshold of the output inverters are at half the supply voltage:

Given

$$V_{dd} - 3 \cdot V_{th} = \frac{V_{dd}}{2}$$

$V_{dd} := \text{Find}(V_{dd})$ $V_{dd} = 1.8\,V$

Part b:



From the memory cell to node X, the time constant is:

$\tau_1 = R \cdot 3 \cdot C_d$

From node X to node Y:

$\tau_2 = R \cdot (2 \cdot C_d + C_{inv})$

From the cin to node Z (assuming that this signal is also used to generate the complement of outc):

$\tau_3 = R \cdot (C_d + 2 \cdot C_g)$

From the memory cell to node W:

$\tau_4 = R \cdot (2C_d + 2C_g)$

It can be seen that the worst case delay will be from cin to the output:

$t = K_2 \cdot \tau_2 + K_3 \cdot \tau_3 + K_4 \cdot \tau_4 + t_{inv}$

Since node X only goes to Vdd - Vtn:

$$K_2 = \ln\left[\frac{V_{dd} - V_{tn}}{\left(V_{dd} - V_{tn}\right) - \frac{V_{dd}}{2}}\right]$$

$$K_3 = K_4 = \ln(2)$$

If we assume that the gate capacitances dominate, then the transistors which are driving gates should be made wider, to reduce their channel resistance, and transistors whose gates are driven by other pass gates should be smaller to reduce their gate capacitances.

Part c:

Since the input to the inverter loses 3 threshold voltages, the inverter PMOS cannot be fully turned off, thus resulting in static current flowing, increasing the total power dissipation.

Part d:

To prevent the 3 threshold voltage drop at the input of the inverter, transmission gates could be used.

This presents increased input capacitances to the driving gates, as well as increased silicon area, and potentially, more S/D leakage due to increased transistor count.

To eliminate the static power consumed by the inverter due to the partially "on" PMOS, a keeper can be introduced at the input of the inverter, controlled by the inverter output.

This approach can result in increased inverter input and output loading due to the added PMOS pull-up. Additional sizing constraints are also introduced into the pass transistor chain design to make sure the inverter input node can be pulled down to ground.

Part e:

Decreasing the threshold voltages would result in less static power dissipation in the output inverters, as well as an increase in dynamic power due to the larger voltage swings at the output of the pass transistors.

In addition, if the threshold voltages are made sufficiently low making the transistors harder to turn off, then current can flow through "sneak paths" formed. Due to the bidirectional nature of the pass transistors, current flow is not limited from the input to the output but also in the reverse direction.