UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

Jan M. Rabaey **Homework 3** **NTU 6342 / EECS 241**
Spring 2007

Note: This is an individual assignment. For problem 1, please attach zoom-in plots from SPICE simulation, as well as the SPICE input files.
Due: March 16 (Friday) via email or post.

1. Dynamic Voltage Scaling Analysis

Consider a FO4 inverter chain of a length of 20.

a) Using HSPICE simulations in 65nm technology, plot its power dissipation vs. operating frequency when the cycle time changes from 20FO4 to 100FO4, with constant supply voltage V_{DD} = 1.1V. The unit inverter is sized 0.5μm/0.25μm with minimum channel lengths.
b) Repeat the simulation from a) for the same inverter chain in the same frequency range, but this time adjust the supply voltage for each frequency such that the power dissipation is minimized. Plot this curve on the same diagram with part a).
c) Repeat the simulation from a) for the same inverter chain in the same frequency range, but this time adjust the substrate biasing while keeping the constant supply V_{DD} = 1.1V. Plot this curve on the same diagram with parts a) and b).
d) Repeat the simulation from a) for the same inverter chain in the same frequency range, but this time adjust both the supply and substrate biasing to minimize power. Plot this curve on the same diagram with parts a), b) and c). How do you determine optimal supplies and thresholds for given frequency in this case?

2. Evaluation of Adiabatic Circuits

Read the paper "Evaluation of Charge Recovery Circuits in Adiabatic Switching for Low Power CMOS Design" by T. Indermaur and M. Horowitz, *1994 IEEE Symposium on Low Power Electronics, Digest of Technical Papers*, p102-103, 1994. Answer the following questions.

a) What are the two circuit styles compared in this work? Write down the delay and energy models used in this analysis, and explain why these two types of circuits are both good candidates for low power designs.
b) Explain the comparison results with and without the switching power considered in charge recovery circuit.
c) According to this analysis, which circuit style is more advantageous for low power design? List some applications where you would recommend using voltage scaling design, and some other applications where the charge recovery circuit suits better.