

UNIVERSITY OF CALIFORNIA
College of Engineering
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Homework 4

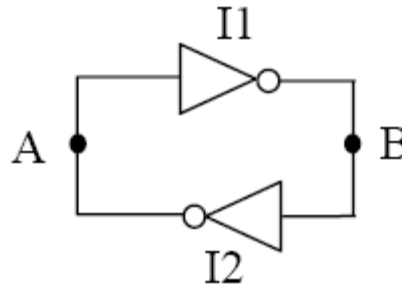
NTU 6342 / EECS 241
Spring 2007

Note: This is an individual assignment. For problem 1, please attach zoom-in plots from SPICE simulation, as well as the SPICE input files.

Due: April 6 (Friday) via email or post.

1. Memory data preservation under ultra-low voltage

Consider a simplified model of memory element circuit as following:



I_1 and I_2 have the same sizes. Assume a 65nm technology. The transistor sizes are $0.12\mu\text{m} / 90\text{nm}$ for PMOS, and $0.2\mu\text{m} / 0.12\mu\text{m}$ for NMOS.

- a) Assume that $A = 1$ is stored at $V_{dd} = 1.1\text{V}$. Use DC analysis in HSPICE simulation, how does the voltages of A and B change when V_{dd} is reduced from 1.1V to zero? At what supply voltage the states are lost? And what happens when V_{dd} is increased from zero to 1.1V again?
- b) Now consider $\pm 8\text{nm}$ process variation in the transistor lengths (both PMOS and NMOS), repeat the simulations in a). What is the highest V_{DD} that the state transition happens, and in what variation scenario?
- c) By modifying the circuit design, can you reduce the V_{DD} value found in b), which is required for the memory data retention in a worst-case variation scenario? Explain how you would modify the circuit and why that helps.

2. Yield and testing

A manufacturing process has yield of 50% (percent of manufactured chips that are good). The manufactured chips are then screened by an acceptance test. Such a test has fault coverage of 90%, which is defined as the percent of faulty chips that are identified as bad (the others are passed because their faults are not detected). All good chips will pass in this test.

- a) What is the percent of passed chips that are defective? What if the fault coverage is increased to 99.9%?
- b) Which is a better way to decrease the per cent of passed chips that are defective; increase yield or increase fault coverage?

3. Timing

A synchronous mixed-signal chip designed to work at 750 MHz has the same clock source, but independent clock trees for the A/D converter (ADC) and digital baseband signal processor. Both clock tree insertion delays are dependent on operating conditions. ADC clock insertion delay is $1.2\text{ns} \pm 0.1\text{ns}$, and the digital clock tree insertion delay is $1.5\text{ns} \pm 0.1\text{ns}$. Additionally, the local skew of both clocks is $\pm 70\text{ps}$. The ADC output register and the receiving flip-flop on the digital side are edge-triggered and have setup times of 70ps, clock-to-output delays of 150ps and 100ps hold times.

Derive the minimum and maximum logic delays for the block of combinational logic between the ADC registers and flip-flops on the digital side.