EE 245 / NEEM 6441: Introduction to MEMS Design
Homework 1: Introduction and Fabrication

1. To pursue your growing interest in MEMS, you decide to attend a conference to learn more about it. For the following conferences, find out:
    a) Five of the major topics covered
    b) How often the conferences are held
    c) Where the most recent one was held
    d) Which you would most like to attend and why

    - International Conference on Solid State Sensors and Actuators (Transducers 07)
    - Solid State Sensor and Actuator Workshop (Hilton Head 06)
    - International Conference on Micro Electro Mechanical Systems (MEMS 07)

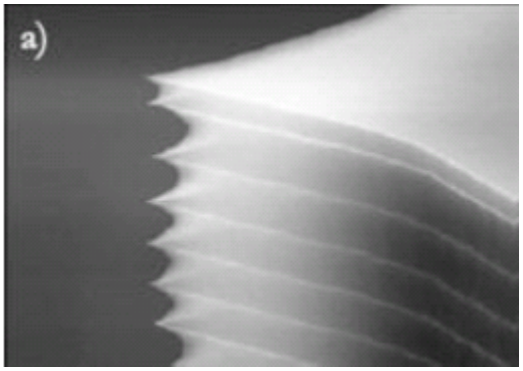
2. Use the SIMPL-er website (also linked from our homework webpage) to view cross-sections of an NMOS transistor.
    - Choose the NMOS transistor process and press "start"
    - Move the horizontal slider back until you are on step 1 and press "calculate cross-section" (you'll have to press this after each step)
    - Move the slider forward one step at a time and press "calculate cross-section" after each step
    - Choose different mask cross sections by clicking on the border of the layout area

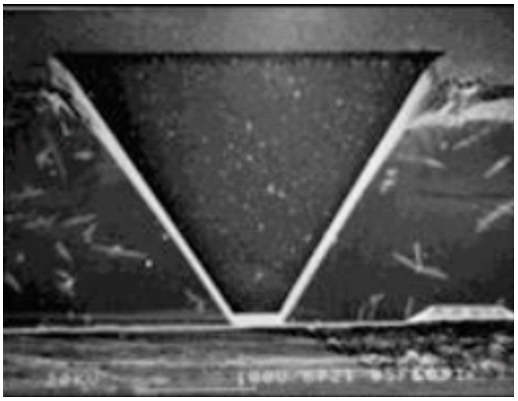
    a) Why doesn't the area under the polysilicon turn green?
    b) What is the point of patterning the oxide in Step 7?

3. For the following structural-sacrificial layer combinations, find the etch rates of the layers using the listed release etchants by consulting the etch tables in Kirt Williams' article, "Etch Rates for Micromachining Processing" (see link on the homework webpage). (Pick the highest etch rate reported for the material and etchant.) For each case calculate :
    - The etch selectivity of the sacrificial material to the structural material
    - The time it would take to etch 1000Å of sacrificial material
    - If the etch selectivity is low (less than 5), suggest a different etchant

	Structural	**Sacrificial**	**Release Etchant**
a)	PolySi (n+)	Annealed PSG 5:1	Buffered HF (BHF)
b)	LTO (undoped)	Si (100)	XeF2 (2.6 torr)
c)	PolySi (undoped)	Nitride (stoichiometric)	SF6 plasma (25 sccm)

4. DRIE is a very common method for dry etching bulk silicon anisotropically. What is going on in the picture at left?





5. KOH provides a method for an anisotropic wet etch of bulk silicon. Consider the picture at right.
    a) Why are these sidewalls sloped?
    b) Calculate (and show your calculation) the angle of the sidewalls relative to the surface of the wafer.

6. Consider the following layout, a simplified version of a MEMS device made at Berkeley. For this problem, assume: positive photoresist, perfectly anisotropic and selective etches (except HF), perfectly isotropic depositions.
    a) Draw the cross section A-A obtained from the following masks after each step in the process listed below.
    b) What is this structure?
    c) What do you think the rectangles on the outside are for?
    d) Why do you think we need the second PSG layer?

    - Start with a flat silicon wafer. Deposit 2 μm PSG.
    - Pattern PSG with mask **ANCH1** (clear field, orange).
    - Deposit 3 μm low-stress nitride (LSN).
    - Pattern nitride with mask **NIT** (dark field, purple).
    - Deposit 1 μm PSG.
    - Pattern PSG with mask **ANCH2** (dark field, blue).
    - Deposit 0.5 μm polysilicon.
    - Pattern polysilicon with mask **POLY** (clear field, green).
    - Release in HF.