1) References:

Lucien J. Breems, Eric J. van der Zwan, E. Carel Dijkmans, Johan H. Huising, "A 1.8mW CMOS ΣΔ Modulator with Integrated Mixer for A/D Conversion of IF signals", ISSCC Digest of Technical papers, pp52,53, Feb 1999

Franz Kuttner, "A 1.2V 10b 20Msample/s Non-Binary Successive Approximation ADC in 0.13µm CMOS", ISSCC Digest of Technical papers, pp 176, 177, Feb 2002

Mikko Waltari, Lauri Sumanen, Tuomas Korhonen, Kari Halonen, "A self-Calibrated Pipeline ADC with 200MHz IF-Sampling Frontend", ISSCC Digest of Technical papers, pp 314,315, Feb 2002

For the Waltari paper:

a) Stated application: cellular base stations (though this is an academic paper so it is not intended for production) In particular, this ADC is meant to digitize multiple channels simultaneously, converting directly from an (under sampled) IF of 200MHz . The idea, then, is to have a fast, very high dynamic range ADC. They present a 13b, 50Msample/s, 200MHz BW pipeline ADC.

b) Function and specification of various blocks (not clear whether these are really specs or just measured results posing as such; see c):

   a. Sample and Hold: Samples the input signal and holds it while the ADC settles. Also provides buffering and a selectable gain of 1 or 2. specs:
      i. Input/output swing: 3.8Vpp differential
      ii. Linearty: not explicitly specified, presumably such that total harmonic distortion <3.8Vpp*2^-13 for Vin=3.8Vpp.
      iii. Noise: not specified but presumably input referred voltage same as above.
      iv. Low jitter clock (since undersampled): again not explicit.

   b. Calibrated, early pipeline stages (2 of them): Each determines 2.5 MSBs by comparing the signal to a reference level and then inserting an appropriate (2 bit) offset. (so together the determine the 4MSBs). Also each gains the signal up to be more easily decoded by the following stage. Finally since slight errors in the inserted offset can result in significant errors farther down the pipeline, a calibration mode is needed to determine the mismatch induced errors in the inserted offsets.

i. Need to provide gain of 4
ii. Low noise (as above)
iii. Programmable offsets of +/- vref *(1/4, ½ and ¾) accurate to one LSB = .01%
iv. these are impossible specs so a calibration is required.

c. Later, uncalibrated pipeline stages (9 of them): Each determines 1.5 bits by comparing the signal to a reference level and then inserting an appropriate (1 bit) offset. (so together the determine the 9LSBs). Also each gains the signal up to be more easily decoded by the following stage.
   i. Gain of 2
   ii. Programmable offsets of +/- vref *(1/4, ½ and ¾) accurate to one LSB*16=0.16%

c) Questions:
   a. Why do they state each stage as having 2.5 or 1.5 bits of resolution: why the .5 part? *I suppose this would be explained in any book or overview article covering pipelined ADCs. (or this class)*

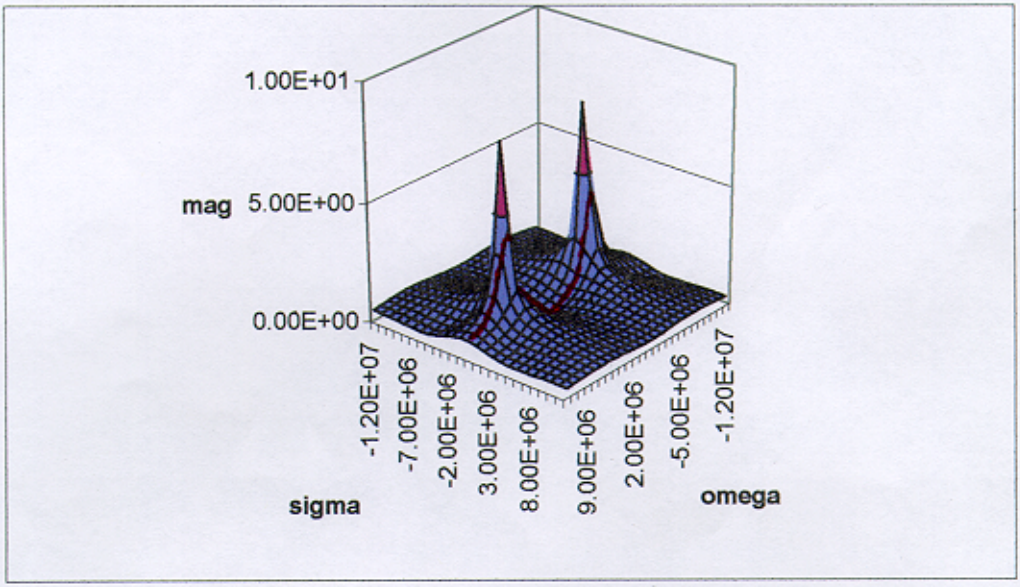
   b. Is it really fair to claim 13 bit resolution when the INL is 3LSBs? *Again this may be in a book or overview. (or this class)*

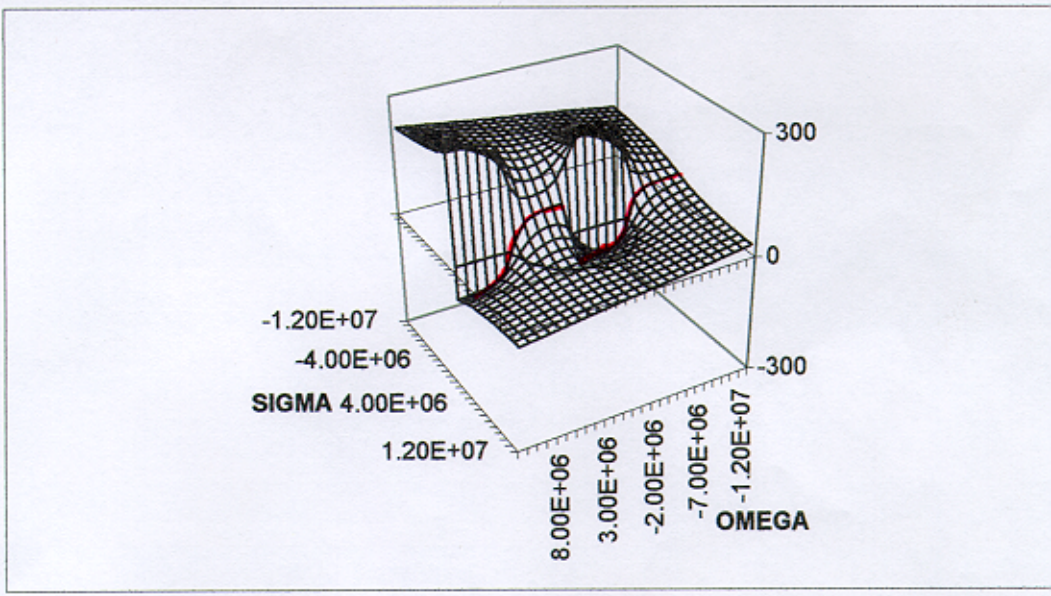
   c. Is 76.5 dB SFDR really good enough for a multi-channel baseband receiver ADC? *This depends on the standard, but the GSM ETSI spec would probably provide enough info to derive the actual specification for an N-channel ADC.*

2) band-pass filter:

a. $\omega p = 2\pi * fc$, $fc = 1MHz$, $wp = 6.28\ Mrad/s$,
$Qp = fp/BW = 1MHz/200kHz = 5$

b. Magnitude and phase on the s-plane for the transfer function:





c) $C = C_1 = C_2 = 1\,pF$

$R = R_1 = R_2 = R_3$

$$\omega_0 = \sqrt{\frac{R_1 + R_2}{R_1 R_2 R_3 C_1 C_2}} = \sqrt{\frac{2R}{R^3 C^2}} = \frac{\sqrt{2}}{RC} = 6.28 \frac{Mrad}{s}$$

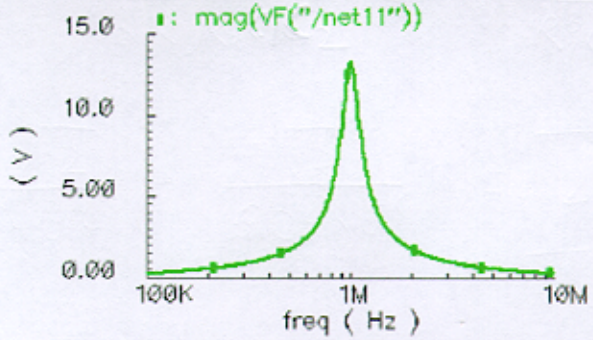
$$R = \frac{\sqrt{2}}{\omega_0 C} = \frac{\sqrt{2}}{6.28 \times 10^{-6}}\,\Omega = \boxed{225\,k\Omega}$$

$$Q_0 = \frac{\omega_0}{\frac{1}{R_1 C_1} + \frac{1}{R_3 C_2} + \frac{1}{R_3 C_1} + \frac{1-K}{R_2 C_1}} = \frac{\omega_0 RC}{4-K} = 5$$

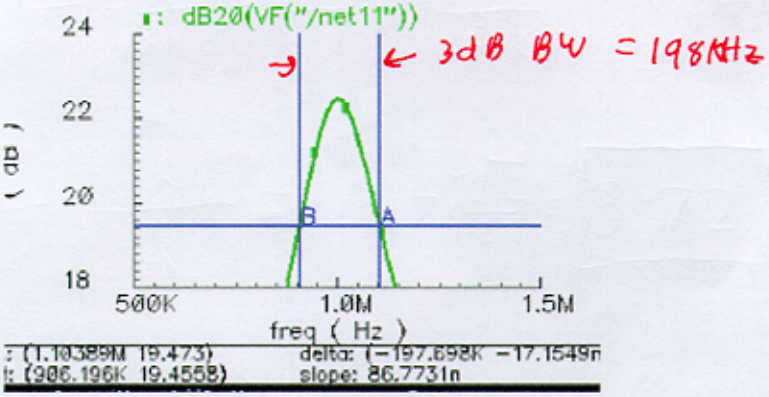
$$K = 4 - \frac{\omega_0 RC}{Q} = 4 - \frac{\sqrt{2}}{5} = \boxed{3.72}$$

$$G = \frac{K/R_1 C_1}{\frac{1}{R_1 C_1} + \frac{1}{R_3 C_2} + \frac{1}{R_3 C_1} + \frac{1-K}{R_2 C_1}} = \frac{K}{4-K} = \boxed{13.28}$$

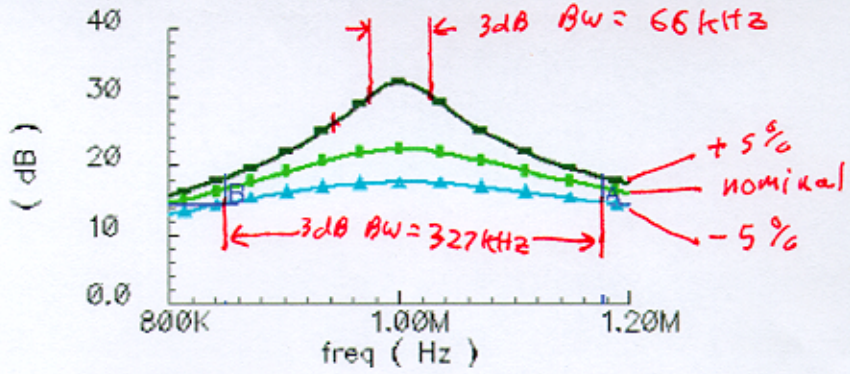
d. As can be seen from simulation, these design values do result in a band pass filter with center frequency of 1MHz and gain of 13.28:



Checking Q, one can see from zooming in that the 3dB bandwidth is almost exactly 200kHz:



Varying K by +/- 5% resulted in Qs of 15 and 3 respectively:



e. Sensitivity of Q to K:

$$S_K^Q = \frac{dQ}{dK} \cdot \frac{K}{Q} = \frac{d}{dK}\left(\frac{RC\omega_0}{4-K}\right) \cdot \frac{K(4-K)}{RC\omega_0}$$

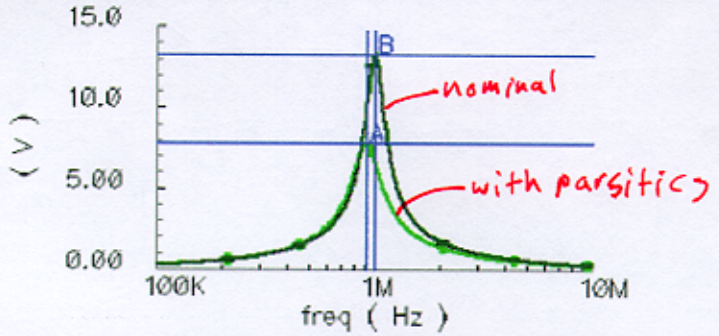
$$= \frac{RC\omega_0}{(4-K)^2} \cdot \frac{K(4-K)}{RC\omega_0}$$

$$= \frac{K}{4-K} = 13.28$$

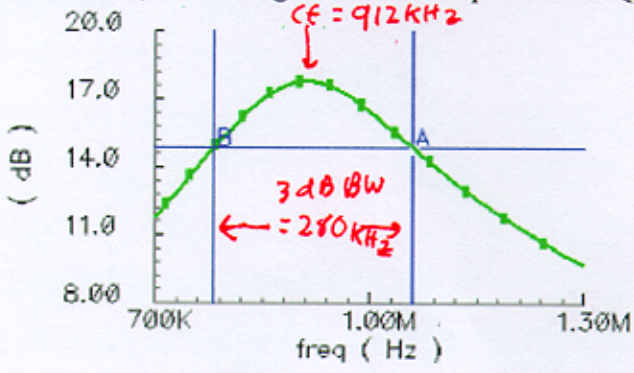
=13.28

This predicts a +/- 66% change in Q for a +/-5% change in K. simulation, however, shows a +300% and –40% change instead. The difference between theoretical and simulated numbers results from the linearity assumption in the theoretical prediction. Since Q is proportional to 1/(4-K), a 5% change in K, changes 4-K by as much as a factor of two, so our linearity assumption is invalid. Simulations of 1% variation in K (not shown) result in Q deviations much closer to that predicted by sensitivity analysis.

f. As can be seen below, adding shunt capacitances of 50fF to both terminals of each cap reduces ωp to 912kHz.



In addition, the adding of the 50fF caps reduces Qp to 912/280 = 3.26:



This is not unexpected given that these parasitics act to effectively increase C1 by 10% as well as add some extra weirdness by shunting R3.