UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Homework 6 **EECS 247**

B.E. Boser
B. Murmann

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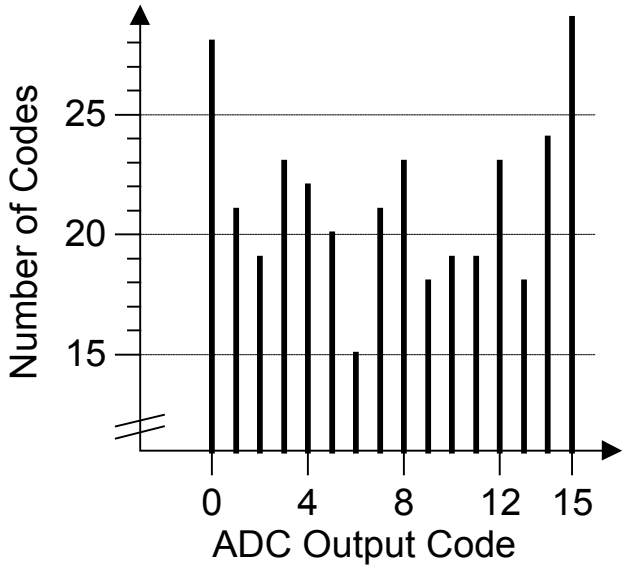
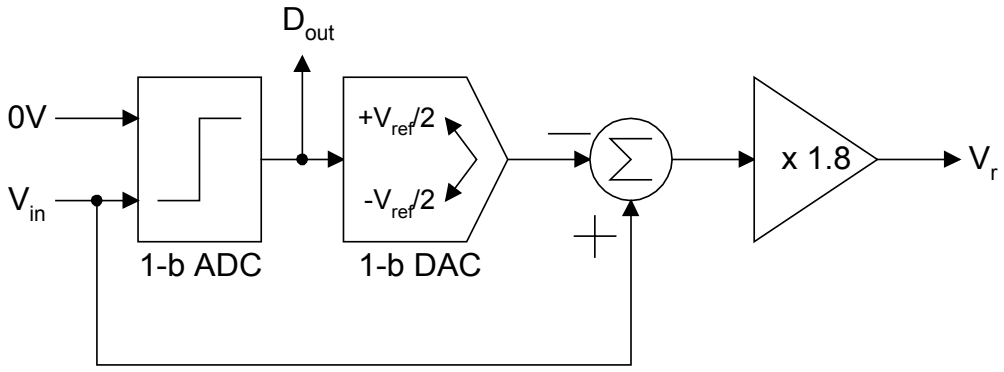
1. An R-string DAC is fabricated with resistors with $\sigma_{\Delta R/R}$=0.2%. For the INL and DNL to be better than 0.5 LSB,
   a) What is the expected yield of a 12-bit DAC?
   b) What is the maximum achievable resolution (no trimming or calibration), if a yield of 99% good parts is desired?

2. The graph below shows a histogram of the output codes obtained for a 4-bit ADC with a linear ramp input. Calculate the peak positive and negative DNL and INL in LSBs.



3. The figure below shows one stage of a radix 1.8 pipeline ADC.
a) Plot V_r as a function of V_{in}/V_{ref}.
b) What is the maximum comparator offset relative to V_{ref} that can be accommodated with digital error correction? Assume everything else is ideal.



4. The sigma-delta modulator below employs and N-bit ADC for increased resolution, but only a 1-bit DAC is used to avoid distortion due to DAC nonlinearity. The remaining N-1 bits serve as an estimate of the quantization error.
a) Draw a linearized schematic which models the quantization error $E_1(z)$ and ADC truncation error $E_2(z)$ as additive white noise sources.
b) Find Y(z) as a function of the input X(z) and the quantization error. What is the optimal value for G?
c) Compute the dynamic range of the converter as a function of N and the oversampling ration M. Assume optimal setting of G and an ideal (i.e. brickwall) decimation filter.