Reference:H:\lib\Mathcad\defaults.mcd

NTU-EECS 247 Midterm Solution Fall 2003 Boris Murmann

1) For an implementation with differentiators, we chose inductor voltages and capacitor currents as state variables

$$I_1 = sC_1(V_2 + V_o)$$

$$V_2 = sL_2\left(\frac{V_o}{R} + I_3\right)$$

$$I_3 = sC_3 \cdot V_o$$

Normalize: $V_1 = I_1 \cdot R$ $V_3 = I_3 \cdot R$ $C_2 = \frac{L_2}{R^2}$

$$V_1 = sRC_1(V_2 + V_o)$$

$$V_2 = sRC_2(V_o + V_3)$$ (Note that Vo is not the same as V3...)

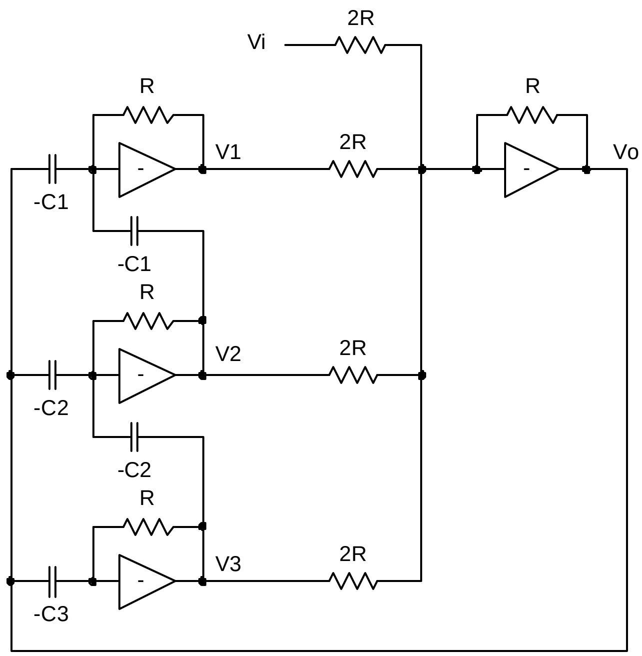
$$V_3 = sRC_3 \cdot V_o$$

Where is the input??? Use KVL, KCL to get:

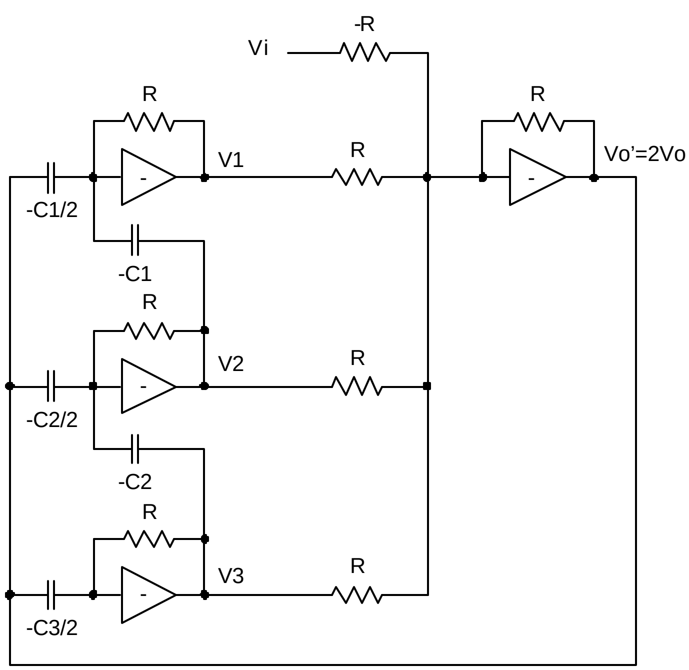
$$V_o = \frac{1}{2} \cdot (V_i - V_1 - V_2 - V_3)$$

Circuit Diagram:

(Looks quite interesting...)



After gain scaling:



2) Worst case alias frequency: $f_a = f_s - 1MHz$

For greater 60dB attenuation: $f_a > 10 \cdot 1MHz$
(One frequency decade)

$f_s - 1MHz > 10MHz$

$\boxed{f_s > 11MHz}$

3)

$f_{out} = 1.25 f_s - f_s$ $\boxed{f_{out} = 0.25fs}$

$$H(s) = \frac{RCs}{1 + 2RCs}$$

$$A_{out} = A \left| H\left(j \cdot 2\pi \cdot f_{out}\right) \right|$$

$$\boxed{A_{out} = A \cdot \frac{RC \cdot 2\pi f_{out}}{\sqrt{1 + \left(2RC \cdot 2\pi f_{out}\right)^2}}}$$

4) Every other code missing - this is the same as a 9-bit ADC, so

$SNR := 6.02 \cdot 9 + 1.76$ $\boxed{SNR = 55.94}$ [dB]

5) Phase1: $Q = V_1 \cdot \left(C_a + C_b\right)$

Phase2: $Q = V_o \cdot C_a + V_2 \cdot C_b$

$$Q = V_1 \cdot \left(C_a + C_b\right) \left| \begin{array}{l} \text{substitute}, Q = V_o \cdot C_a + V_2 \cdot C_b \\ \text{solve}, V_o \end{array} \right. \rightarrow \frac{\left(-V_2 \cdot C_b + V_1 \cdot C_a + V_1 \cdot C_b\right)}{C_a}$$

$$\boxed{V_o(z) = V_1 \cdot \left(1 + \frac{C_b}{C_a}\right) \cdot z^{\frac{-1}{2}} - V_2 \cdot \frac{C_b}{C_b}}$$