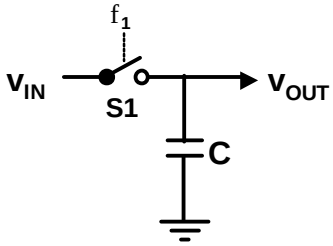
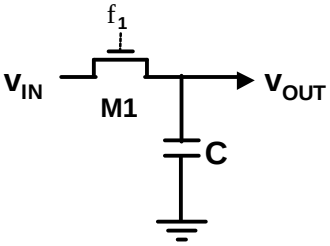
Sampling

Ideal Sampling



- Grab exact value of V_{in} when switch opens

Practical Sampling



- kT/C noise
- Finite R_{sw} → limited bandwidth
- $R_{sw} = f(V_{in})$ → distortion
- Switch charge injection (EE240)
- Clock jitter

kT/C Noise

$$\frac{k_B T}{C} \leq \frac{\Delta^2}{12}$$

$$C \geq 12 k_B T \left(\frac{2^B - 1}{V_{FS}} \right)^2$$

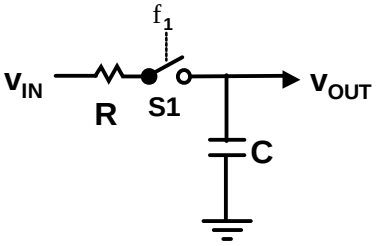
In high resolution ADCs kT/C noise usually dominates overall error (power dissipation argument).

B	C_{min} (V_{FS} = 1V)
8	0.003 pF
12	0.8 pF
14	13 pF
16	206 pF
20	52,800 pF

Acquisition Bandwidth

- The resistance R of switch S1 turns the sampling network into a lowpass filter with risetime = RC = τ
- Assuming V_{in} is constant during the sampling period and C is initially discharged (a good idea—why?):

$$v_{out}(t) = v_{in}\left(1 - e^{-t/t}\right)$$



Switch On-Resistance

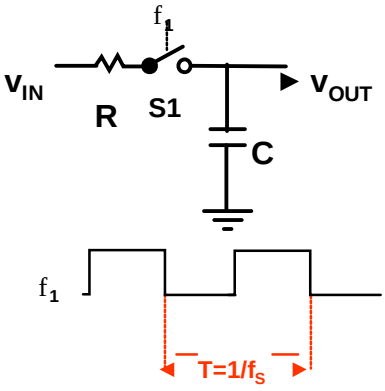
$$v_{in} - v_{out}\left(t = \frac{1}{2f_s}\right) << \Delta$$

$$v_{in} e^{-\frac{1}{2}f_s t} << \Delta$$

$$\text{Worst Case}: \quad v_{in} = V_{FS}$$

$$t << -\frac{T}{2}\frac{1}{\ln\left(2^B - 1\right)}$$

$$R << -\frac{1}{2f_s C}\frac{1}{\ln\left(2^B - 1\right)}$$



Example:

B = 14, C = 13pF, f_s = 100MHz

T/τ >> 19.4, R << 40Ω

Switch On-Resistance

$$I_{D(triode)} = mC_{ox}\frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}$$

$$\frac{1}{R_{ON}} \cong \left.\frac{dI_{D(triode)}}{dV_{DS}}\right|_{V_{DS}\to 0}$$

$$= \frac{1}{mC_{ox}\frac{W}{L}(V_{GS} - V_{TH})}$$

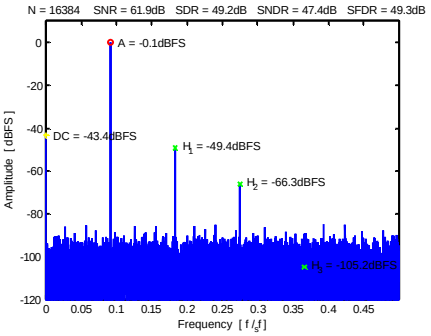
$$= \frac{1}{mC_{ox}\frac{W}{L}(V_{DD} - V_{TH} - v_{in})}$$

$$= \frac{1}{R_o}\frac{1}{1-\frac{v_{in}}{V_{DD}-V_{TH}}} \qquad \text{with} \qquad R_o = \frac{1}{mC_{ox}\frac{W}{L}(V_{DD} - V_{TH})}$$

$$R_{ON} = R_o\left(1-\frac{v_{in}}{V_{DD}-V_{TH}}\right)$$

Sampling Distortion

$$v_{out} = v_{in}\left(1 - e^{-\frac{T}{2t}\frac{1}{1-\frac{v_{in}}{V_{DD}-V_{TH}}}}\right)$$

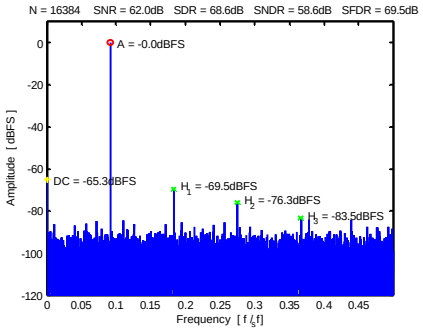


$T/\tau = 10$

$V_{DD} - V_{TH} = 2V$ $V_{FS} = 1V$

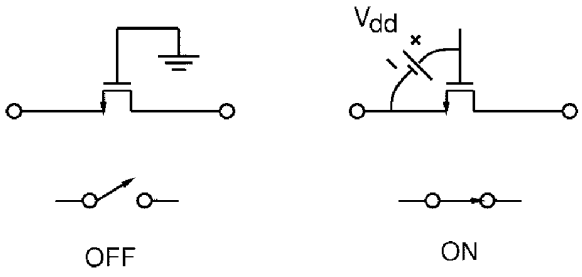
Sampling Distortion

- SFDR is very sensitive to sampling distortion
- Solutions:
  - Overdesign switches
    → increased switch charge injection
  - Complementary switch
  - Maximize V_{DD}/V_{FS}
    → increased noise
  - Constant V_{GS} ? $f(V_{in})$
    → …



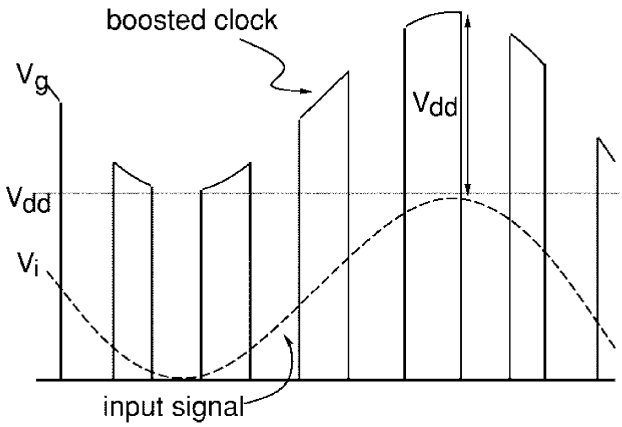
T/τ = **20**
$V_{DD} - V_{TH}$ = 2V V_{FS} = 1V

Constant V_{GS} Sampling

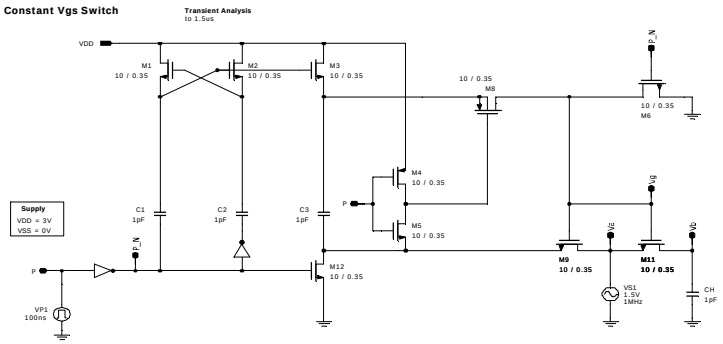


- Switch overdrive voltage is independent of signal
- Error from finite R_{ON} is linear (to first order)

Constant V_{GS} Sampling

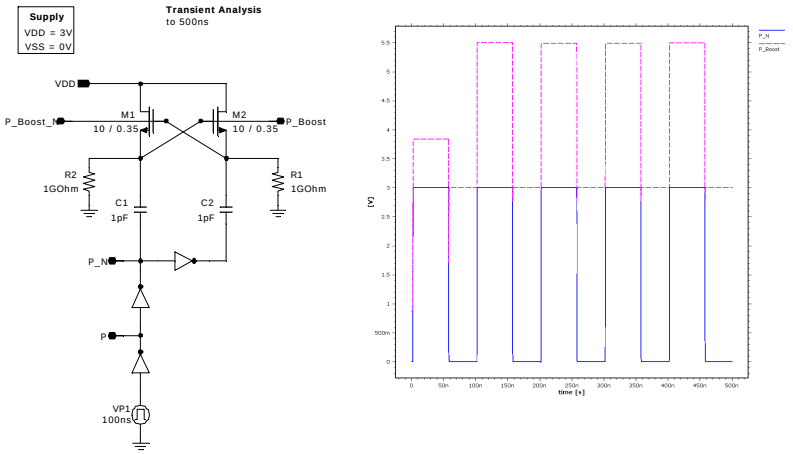


Constant V_{GS} Sampling Circuit



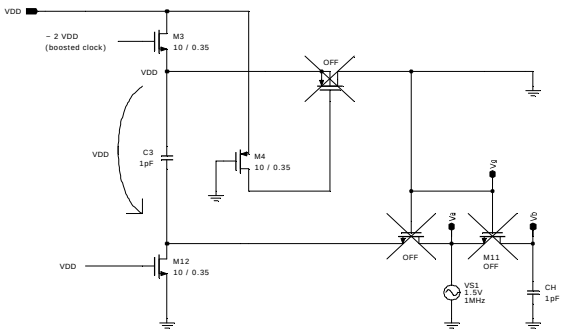
Clock Multiplier

Clock Booster



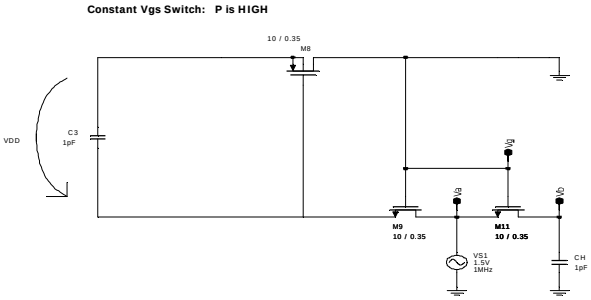
Constant V_{GS} Sampler: Φ LOW

Constant Vgs Switch: P is LOW



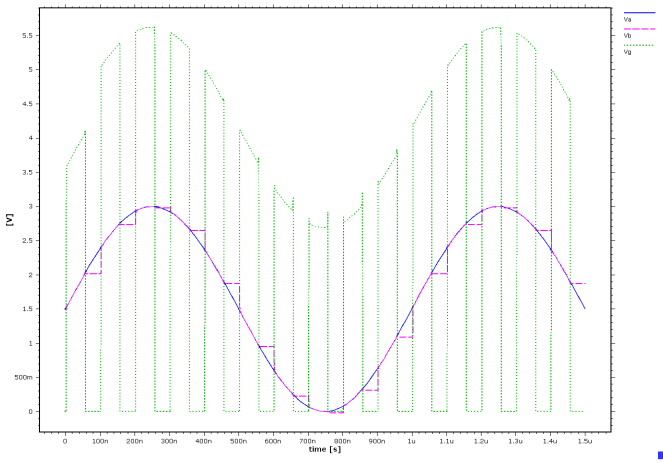
- Sampling switch M11 is OFF
- C3 charged to VDD

Constant V_{GS} Sampler: Φ HIGH

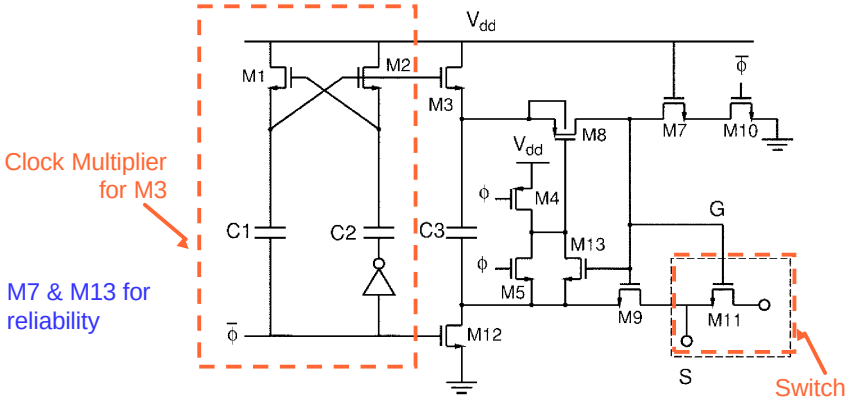


- C3 previously charged to VDD
- M8 & M9 are on: C3 across G-S of M11
- M11 on with constant VGS = VDD

Constant V_{GS} Sampling

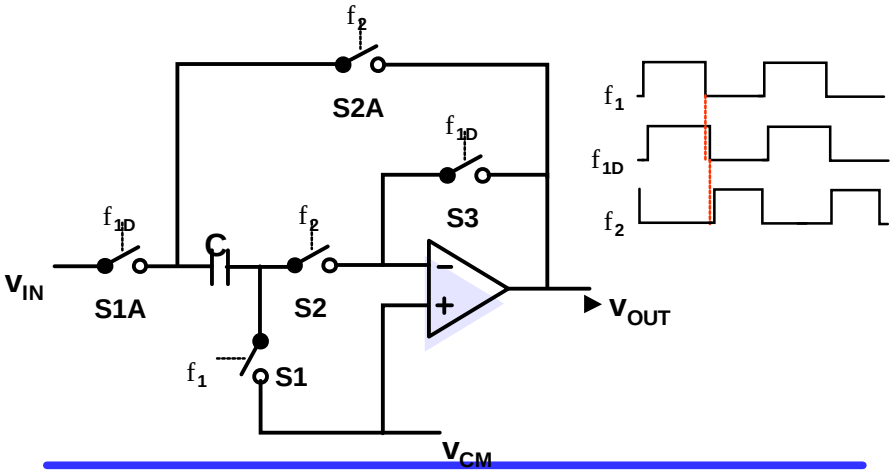


Complete Circuit

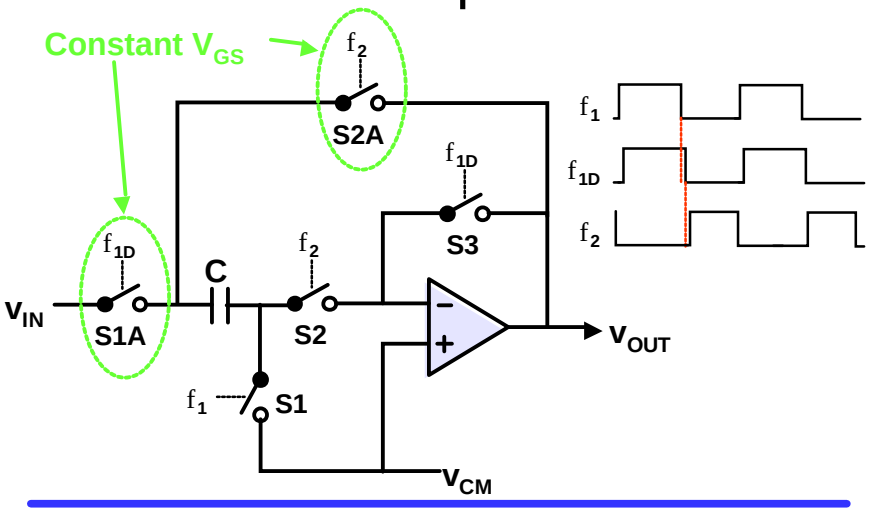


Ref: A. Abo et al, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," JSSC May 1999, pp. 599.

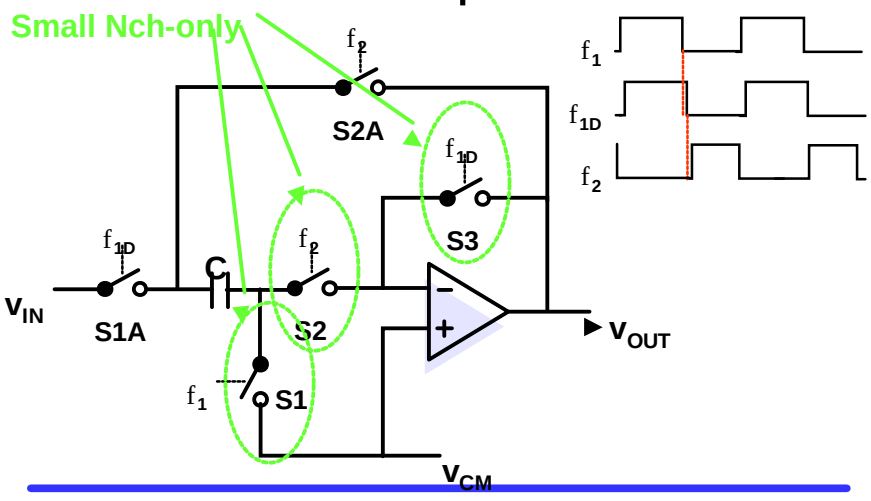
CMOS Sample & Hold



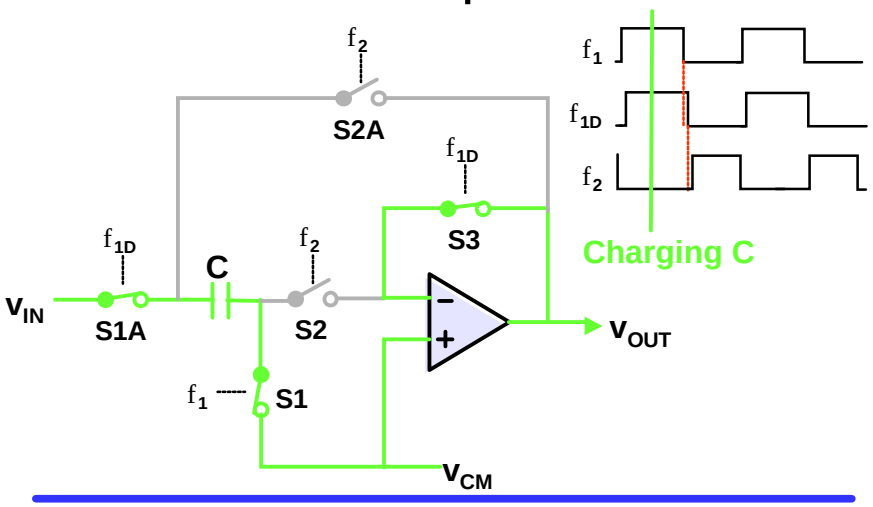
CMOS Sample & Hold



CMOS Sample & Hold



CMOS Sample & Hold



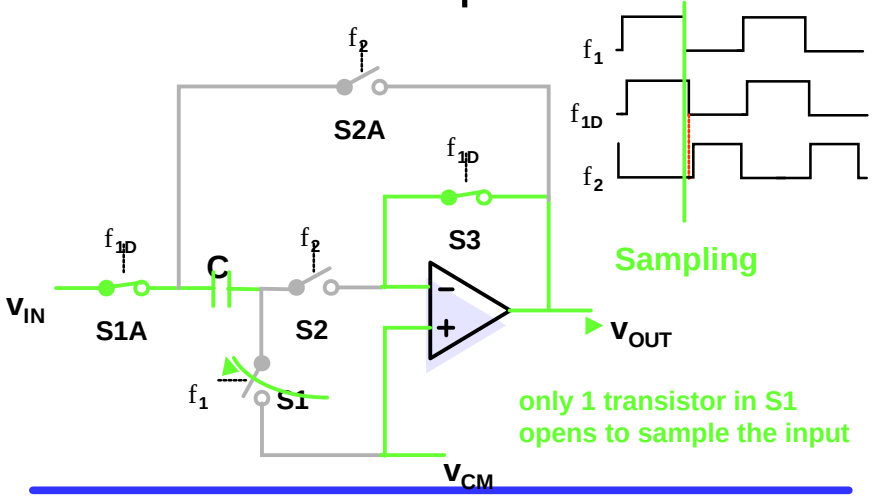
CMOS Sample & Hold

- S1 is an n-channel MOSFET
- S1 provides as much of the sampling path resistance as possible ($R=R_{S1A}+R_{S1}$)
  - S1A is a wide (much lower resistance than S1) constant V_{GS} switch
  - If S1A's resistance is negligible, aperture delay depends only on S1 resistance
  - S1 resistance is independent of v_{IN}; hence, aperture delay is independent of v_{IN}

Charge Injection

- At the instant of sampling, some of the charge stored in sampling switch S1 is dumped onto C
  - This unwanted charge is called “charge injection”
- The circuit on slide 15.2 has charge injection that varies in a wildly nonlinear fashion with v_{IN}
- With the CMOS Sampling Circuit, charge injection comes only from S1 and is first-order independent of v_{IN}
  - Only a dc offset is added to the input signal
  - This dc offset can be removed with a differential architecture

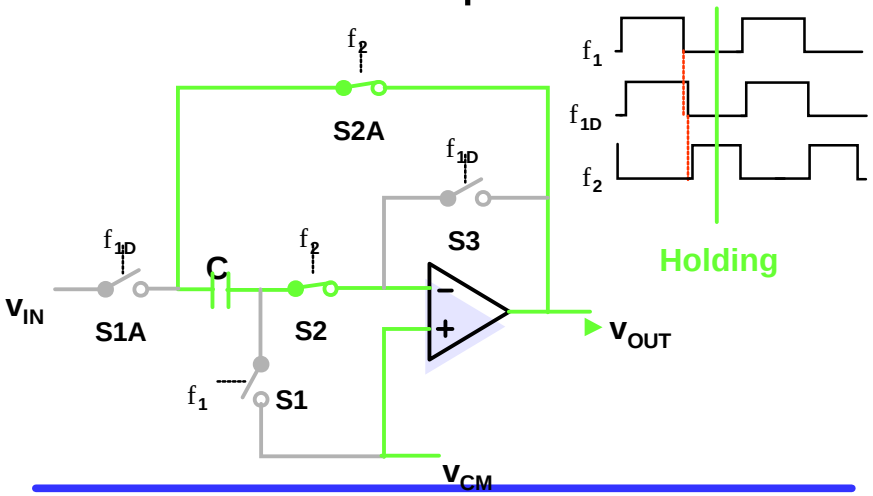
CMOS Sample & Hold



CMOS Sample & Hold

- During ϕ_2, the opamp buffers the sampling capacitor for loads that need it
- The hold topology is shown on the following slide…

CMOS Sample & Hold

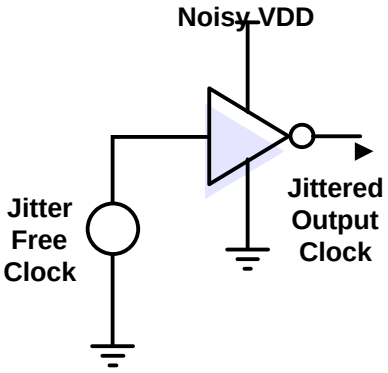


Jitter

- All of the preceding analyses assume that sampling impulses are spaced evenly in time
- In the real world, separation of sampling impulses has some distribution around the nominal value T
- The variability in T is called jitter

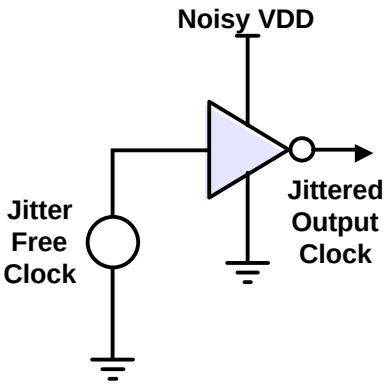
Jitter

- The dominant cause of clock jitter in most chips is power supply noise produced by unrelated activity in other parts of the chip
- The inverter symbol represents a chain of gates in the sampling clock path



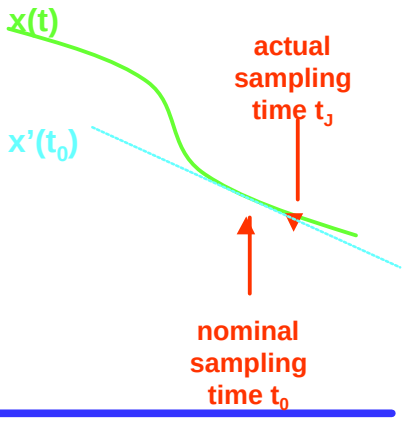
Jitter

- Let's assume the inverter delay is 100psec, and that the delay varies by 20% per volt change in VDD (20psec/V)
- 200mV of power supply noise becomes 4psec of clock jitter



Jitter

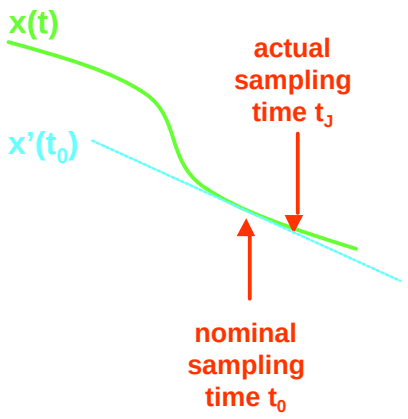
- Sampling jitter adds an error voltage proportional to the product of (t_J-t_0) and the derivative of the input signal at the sampling instant
- Jitter doesn't matter when sampling dc signals



Jitter

- The error voltage is

$$e = x'(t_0)(t_J - t_0)$$



Jitter Example

Sinusoidal input

Amplitude : A

Frequency : f_x

Jitter : $?t$

$$x(t) = A\sin(2pf_x t)$$
$$x'(t) = 2pfA\cos(2pf_x t)$$
$$|x'(t)| \le 2pfA$$
$$|e(t)| \le |x'(t)|?t$$

Worst case

$$A = A_{FS}$$
$$f_x = f_s/2$$
$$|e(t)| << \frac{\Delta}{2} \cong \frac{A_{FS}}{2^{B+1}}$$
$$?t << \frac{1}{2^B p f_s}$$

B	f_s	Δt << than
16	10 MHz	0.5 ps
12	100 MHz	0.8 ps
8	1000 MHz	1.2 ps

The Jitter Law

- The worst case looks pretty stringent …
  what about the "average"?
- Let's calculate the mean squared jitter error (variance)
- If we're sampling a sinusoidal signal

  $x(t) = A\sin(2\pi f_x t)$,

  then
  - $x'(t) = 2\pi f_x A\cos(2\pi f_x t)$
  - $E\{[x'(t)]^2\} = 2\pi^2 f_x^2 A^2$
- If jitter is uniformly distributed from $-\tau/2$ to $+\tau/2$
  - $E\{(t_J - t_0)^2\} = \tau^2/12$

The Jitter Law

- If $x'(t)$ and the jitter are independent
  - $E\{[x'(t)(t_J - t_0)]^2\} = E\{[x'(t)]^2\}\, E\{(t_J - t_0)^2\}$
- Hence, the jitter error power is

$$\mathbf{E\{e^2\} = p^2 f_x^2 A^2 t^2/6}$$

- If the jitter is uncorrelated from sample to sample, this "jitter noise" is white

The Jitter Law

$$DR_{\text{jitter}} = \frac{A^2/2}{p^2 f_x^2 A^2 t^2/6} = \frac{3}{p^2 f_x^2 t^2} = -20\log_{10}(f_x t) - 5.172\text{dB}$$

f_x	τ	DR_{jitter}	ENOB
1 MHz	1 ns	55 dB	8.8
1 MHz	2 ps	109 dB	17.8
100 MHz	0.4 ps	83 dB	13.5
1000 MHz	0.5 ps	61 dB	9.8

The Jitter Law

- The Jitter Law must be respected whenever you require high-resolution conversion of high frequency signals
  - Sampling a 1MHz signal with 1nsec of peak-to-peak jitter yields a dynamic range of only 55dB
- In practice, jitter is usually controlled to add negligible to the total converter error (i.e. thermal and quantization noise)
- This translates into the jitter being ~10dB below other noise sources
  - For 16 Bit conversion of 1MHz signals, a –109dB jitter DR limit requires < 2 psec peak-to-peak jitter

The Jitter Law

- Clock jitter in the single-digit picosecond range doesn't just happen
  - Separate supplies
  - Separate analog and digital clocks
  - Short inverter chains between clock and sampling switch
- Few, if any, other analog-to-digital conversion nonidealities have the same symptoms as sampling jitter:
  - RMS noise proportional to input frequency
  - RMS noise proportional to input amplitude
- So, if sampling clock jitter is limiting your dynamic range, it's easy to tell, but difficult to fix
  - Very difficult to fix in silicon without all-layer mask revisions