D/A Converters

- D/A architecture examples
  - Unit element
  - Binary weighted
- Static performance
  - Component matching
  - Architectures
    - Unit element
    - Binary weighted
    - Segmented
  - Dynamic element matching
- Dynamic performance
  - Glitches
  - Reconstruction filter
- DAC Examples

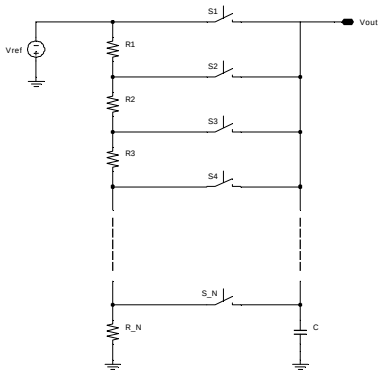
D/A Examples

- Voltage, Charge, or Current Based
- E.g.
  - Resistor string
  - Charge redistribution
  - M-DAC

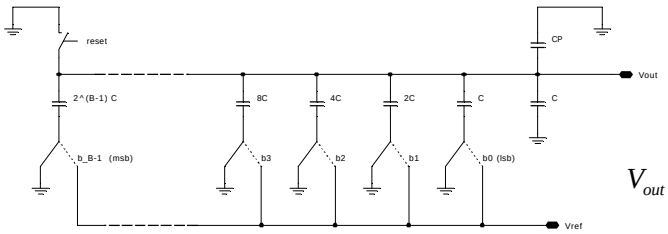
R-String DAC

- "Unit element"
- Inherently monotonic
- 2^B resistors and 2^B switches for B bits
- Simple and relatively fast up to ~ 10 bits
- High element count, settling time for B > 10: $\tau = 0.25 \times 2^B RC$

- Ref: M. Pelgrom, "A 10-b 50-MHz CMOS D/A Converter with 75-W Buffer," JSSC, Dec. 1990, pp. 1347.



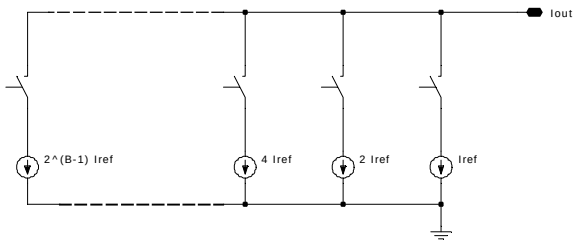
Charge Redistribution DAC



$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C + C_P} V_{ref}$$

- "Binary weighted"
- Monotonicity depends on element matching
- B+1 capacitors (2^B unit elements)

M-DAC



- "Binary weighted"
  Often realized with unit elements also
- Monotonicity depends on element matching
- B current sources (2^B-1 unit elements)

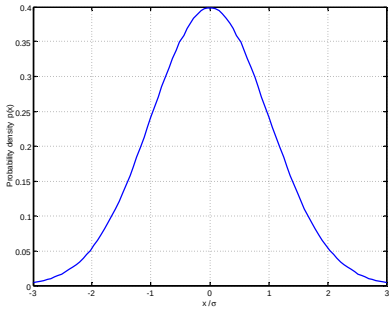
Static DAC INL / DNL Errors

- Component Matching
- Systematic Errors
  - Contact resistance
  - Edge effects in capacitor arrays
  - Process gradient
  - Finite current source output resistance
- Random Errors
  - Lithography
  - Often Gaussian distribution (central limit theorem)

C. Conroy et al, "Statistical Design Techniques for D/A Converters," JSSC Aug. 1989, pp. 1118-28.

Gaussian Distributions

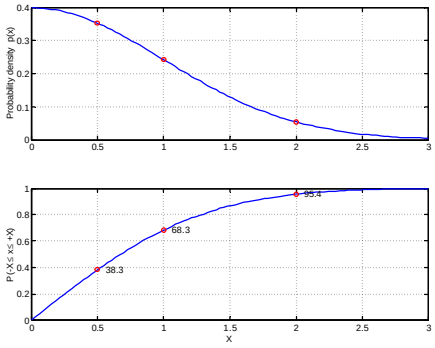
$$p(x) = \frac{1}{\sqrt{2p}\,s} e^{-\frac{(x-m)^2}{2s^2}}$$



Yield

$$P(-X \le x \le +X) = \frac{1}{\sqrt{2p}} \int_{-X}^{+X} e^{-\frac{x^2}{2}} dx$$

$$= \mathrm{erf}\left(\frac{X}{\sqrt{2}}\right)$$



Yield

X/s	P(-X £ x £ X) [%]	X/s	P(-X £ x £ X) [%]
0.2000	15.8519	2.2000	97.2193
0.4000	31.0843	2.4000	98.3605
0.6000	45.1494	2.6000	99.0678
0.8000	57.6289	2.8000	99.4890
1.0000	68.2689	3.0000	99.7300
1.2000	76.9861	3.2000	99.8626
1.4000	83.8487	3.4000	99.9326
1.6000	89.0401	3.6000	99.9682
1.8000	92.8139	3.8000	99.9855
2.0000	95.4500	4.0000	99.9937

Example

- Measurements show that the offset voltage of a batch of operational amplifiers follows a Gaussian distribution with $\sigma = 2mV$ and $\mu = 0$.
- Fraction of opamps with $|V_{os}| < X = 6mV$:
  - $X/\sigma = 3$ → 99.73 % yield (we'd still test before shipping!)
- Fraction of opamps with $|V_{os}| < X = 400\mu V$:
  - $X/\sigma = 0.2$ → 15.85 % yield

DNL Unit Element DAC

E.g. Resistor string DAC:

$$\Delta = R_o I_{\text{ref}}$$

$$\Delta_i = R_i I_{\text{ref}}$$

$$DNL_i = \frac{\Delta_i - \Delta}{\Delta}$$

$$= \frac{R_i - R_o}{R_o} = \frac{\Delta R_i}{R_o} \approx \frac{\Delta R_i}{R_i}$$

$$s_{DNL} = s_{\frac{\Delta R_i}{R_i}}$$

DNL of unit element DAC is independent of resolution!

Example:

If $\sigma_{\Delta R/R}$ = 1%, what DNL spec goes into the datasheet so that 99.9% of all converters meet the spec?

Answer:

From table: X/σ = 3.3

$\sigma_{DNL} = \sigma_{\Delta R/R}$ = 1%

3.3 σ_{DNL} = 3.3%

→ +/- 0.033 LSB

DAC INL

- Error is maximum at mid-scale:

$$s_{INL} = \frac{1}{2}\sqrt{2^B - 1}\, s_e$$

$$\text{with } N = 2^B - 1$$

- Depends on DAC resolution and element matching σ_ε

Ref: Kuboki et al, TCAS, 6/1982

Untrimmed DAC INL

$$s_{INL} \cong \frac{1}{2}\sqrt{2^B - 1}\, s_e$$

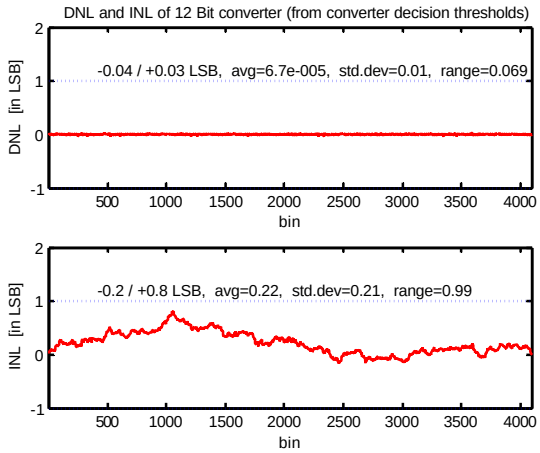
$$B \cong 2 + 2\log_2\left[\frac{s_{INL}}{s_e}\right]$$

Example:

σ_{INL} = 0.1 LSB

σ_ε = 1%	B = 8.6
σ_ε = 0.5%	B = 10.6
σ_ε = 0.2%	B = 13.3
σ_ε = 0.1%	B = 15.3

Simulation Example



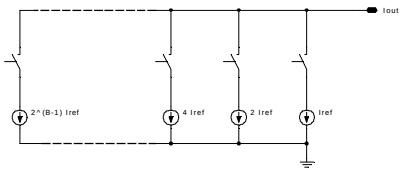
σ_ε = 1%
B = 12

σ_{INL} = 0.3 LSB (midscale)

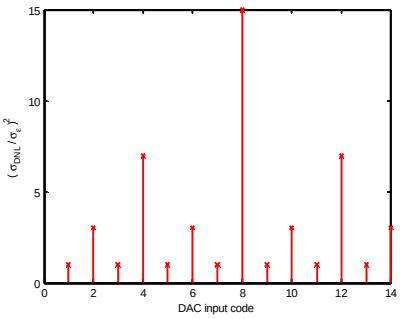
Binary Weighted DAC

- INL same as for unit element DAC
- DNL depends on transition
- Consider
  0111 … → 1000 …

Sample realization of binary weighted DAC:



DNL of Binary Weighted DAC

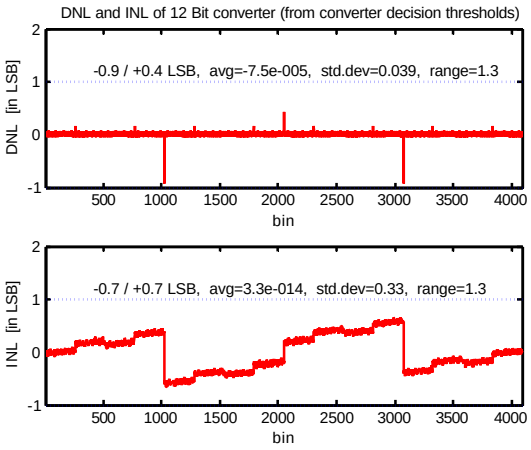


- Worst-case transition occurs at mid-scale:

$$s_{DNL}^2 = \underbrace{\left(2^{B-1}-1\right)s_e^2}_{0111\ldots} + \underbrace{\left(2^{B-1}\right)s_e^2}_{1000\ldots}$$
$$\cong 2^B s_e^2$$

- Example:
  B = 12, σ_ε = 1%
  → σ_{DNL} = 0.64 LSB

Simulation Example

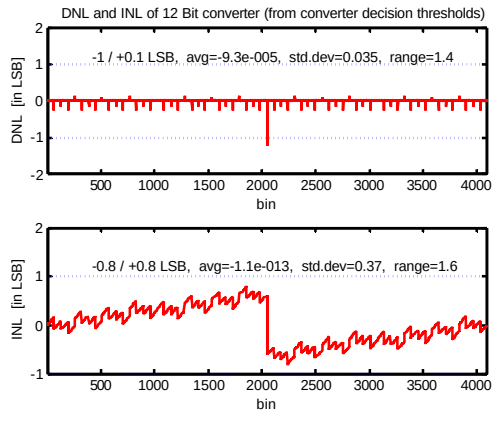


σ_ε = 1%
B = 12

σ_{DNL} = 0.6 LSB (midscale)

MSB transitions clearly visible

"Another" Random Run …



Now (by chance) worst DNL is mid-scale.

Statistical result!

Unit Element vs Binary Weighted

Unit Element DAC	Binary Weighted DAC
$s_{DNL} = s_e$	$s_{DNL} \cong 2^{B/2} s_e = 2 s_{INL}$
$s_{INL} \cong 2^{B/2-1} s_e$	$s_{INL} \cong 2^{B/2-1} s_e$

Number of switched elements:

$S = 2^B$	$S = B$

Significant difference in performance and complexity!

DAC INL/DNL Summary

- DAC architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results are for uncorrelated random element variations
- Systematic errors and correlations are usually also important

Ref: Kuboki, S.; Kato, K.; Miyakawa, N.; Matsubara, K. Nonlinearity analysis of resistor string A/D converters. IEEE Transactions on Circuits and Systems, vol.CAS-29, (no.6), June 1982. p.383-9.

Segmented DAC

- Objective:
  compromise between unit element and binary weighted DAC
- Approach:
  B_1 MSB bits → unit elements
  $B_2 = B\text{-}B_1$ LSB bits → binary weighted
- INL: unaffected
- DNL: worst case occurs when LSB DAC turns off and one more MSB DAC element turns on: same as binary weighted DAC with B_2+1 bits
- Switched Elements: $(2^{B1}\text{-}1) + B_2$

Comparison

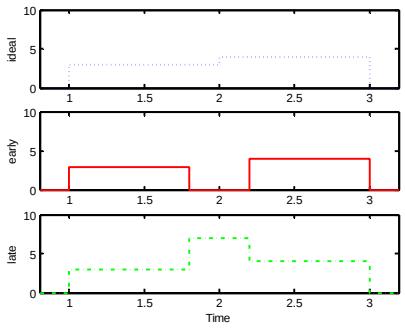
Example:

B = 12, $B_1 = 5$, $B_2 = 7$
$\sigma_\varepsilon = 1\%$

DAC Architecture	σ_{INL}	σ_{DNL}	# s.e.
Unit element	0.32	0.01	4095
Binary weighted	0.32	0.64	12
Segmented	0.32	0.16	31+7

Dynamic DAC Error: Glitch

- Consider binary weighted DAC transition 011 → 100
- DAC output depends on timing
- Plot shows situation where
  - MSBs switch on time
  - LSBs switch
    - On time
    - Early
    - Late



Glitch Energy

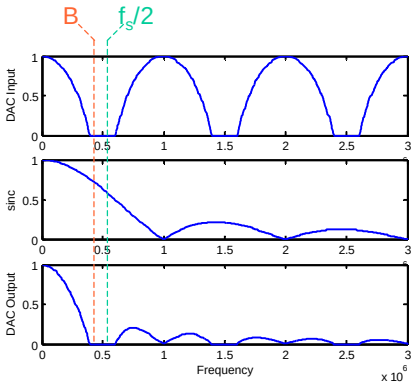
- Glitch energy (worst case): $\Delta t\ 2^{B-1}$
- LSB energy: T
- Need $\Delta t\ 2^{B-1} << T$ or $\Delta t << 2^{-B+1}$
- Examples:

f_s [MHz]	B	Δt [ps]
1	12	<< 488
20	16	<< 1.5
1000	10	<< 2

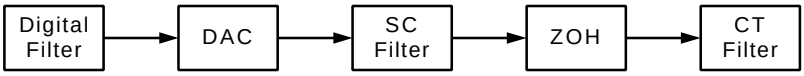
Compare to digital circuit clock skew …

DAC Reconstruction Filter

- Need for and requirements depend on application
- Tasks:
  - Correct for sinc distortion
  - Remove “aliases” (stair-case approximation)



Reconstruction Filter Options



- Digital and SC filter possible only in combination with oversampling (signal bandwidth B << $f_s/2$)
- Digital filter can prewarp spectrum to compensate in-band sinc attenuation (from ZOH)

Sample DAC Implementations

- Untrimmed segmented
  - T. Miki et al, “An 80-MHz 8-bit CMOS D/A Converter,” JSSC December 1986, pp. 983.
  - A. Van den Bosch et al, “A 1-GSample/s Nyquist Current-Steering CMOS D/A Conveter,” JSSC March 2001, pp. 315.
- Current copiers:
  - D. W. J. Groeneveld et al, “A Self-Calibration Techique for Monolithic High-Resolution D/A Converters,” JSSC December 1989, pp. 1517.
- Dynamic element matching:
  - R. J. van de Plassche, “Dynamic Element Matching for High-Accuracy Monolithic D/A Converters,” JSSC December 1976, pp. 795.

An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAO NAKAYA, SOTOJU ASAI, YOICHI AKASAKA, AND YASUTAKA HORIBA

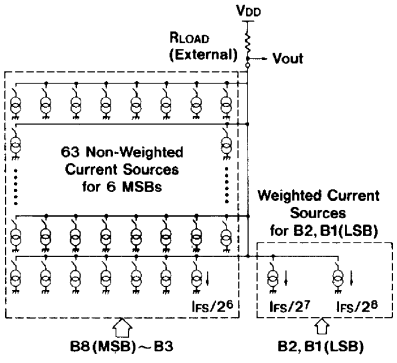


Fig. 1. Basic architecture of the DAC.

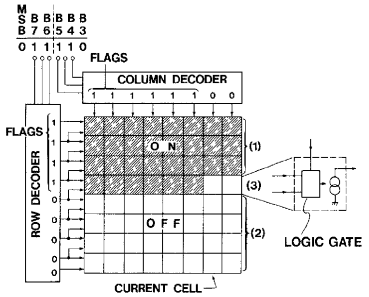
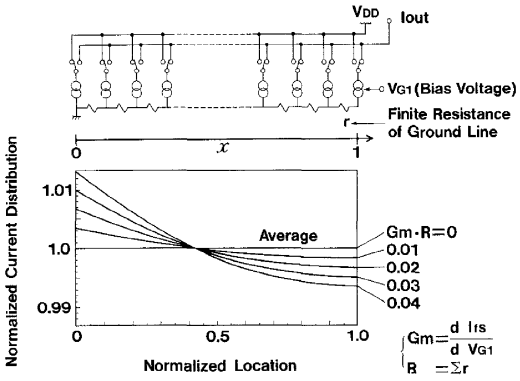


Fig. 2. Two-step decoding.



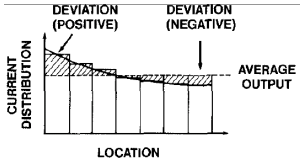
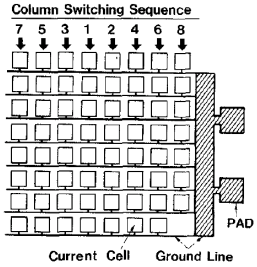
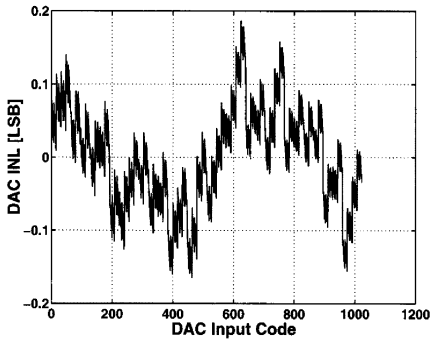


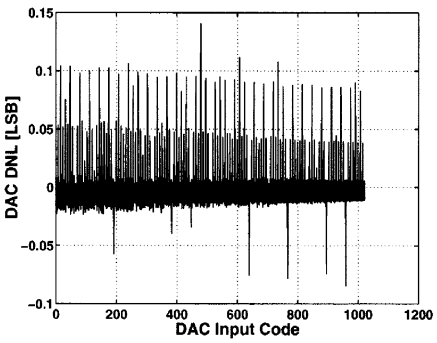
Fig. 9. Symmetrical switching.



A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter

Anne Van den Bosch, *Student Member, IEEE*, Marc A. F. Borremans, *Student Member, IEEE*, Michel S. J. Steyaert, *Senior Member, IEEE*, and Willy Sansen, *Fellow, IEEE*





IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 6, DECEMBER 1989

A Self-Calibration Technique for Monolithic High-Resolution D/A Converters

D. WOUTER J. GROENEVELD, HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, HENK A. H. TERMEER, AND CORNELIS A. A. BASTIAANSEN

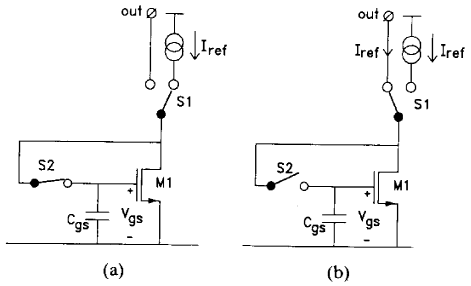
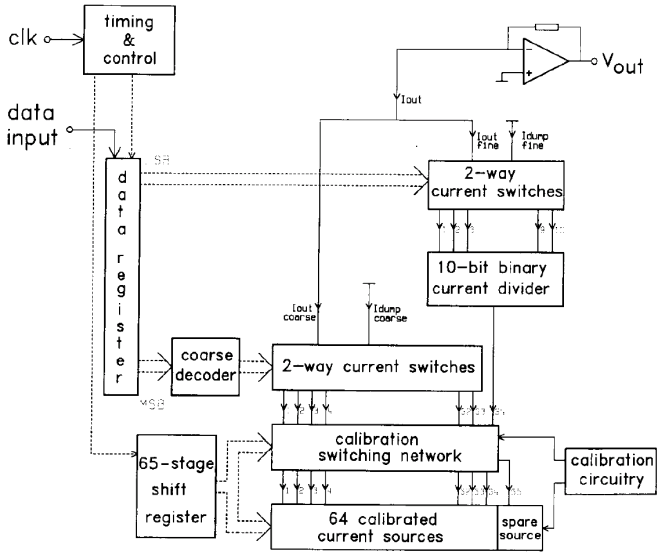
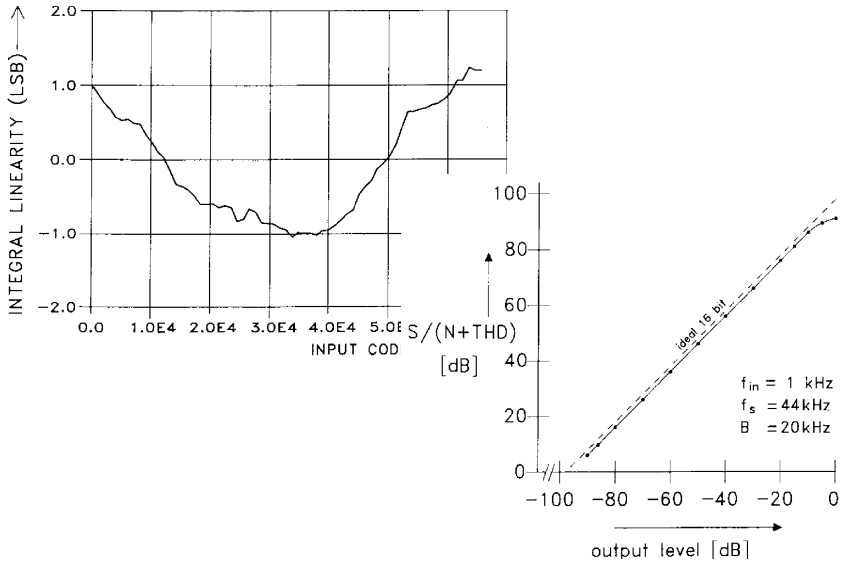


Fig. 2. Calibration principle. (a) Calibration. (b) Operation.





IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-11, NO. 6, DECEMBER 1976 795

Dynamic Element Matching for High-Accuracy Monolithic D/A Converters

RUDY J. VAN DE PLASSCHE

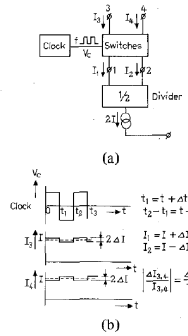


Fig. 2. (a) New current divider schematic diagram. (b) Time dependence of various currents in the new divider.

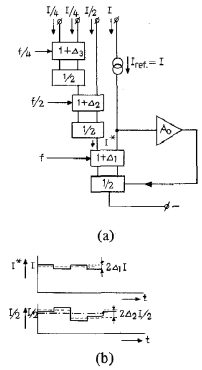
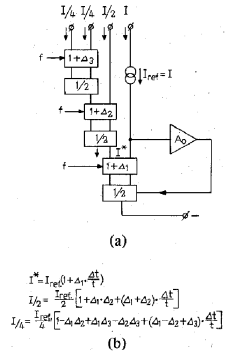


Fig. 4. (a) Binary weighted current network using different switching frequencies. (b) Time dependence of currents flowing in the first and second divider stage.



(a) Binary weighted current network with equal switching frequency. (b) Error analysis results.

Dynamic Element Matching

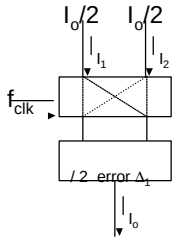
During Φ_1

$$I_1^{(1)} = \tfrac{1}{2} I_o(1+\Delta_1)$$
$$I_2^{(1)} = \tfrac{1}{2} I_o(1-\Delta_1)$$

During Φ_2

$$I_1^{(2)} = \tfrac{1}{2} I_o(1-\Delta_1)$$
$$I_2^{(2)} = \tfrac{1}{2} I_o(1+\Delta_1)$$

$$\langle I_2 \rangle = \frac{I_2^{(1)} + I_2^{(2)}}{2} = \frac{I_o}{2}\frac{(1-\Delta_1)+(1+\Delta_1)}{2} = \frac{I_o}{2}$$



Dynamic Element Matching

During Φ_1

$$I_1^{(1)} = \tfrac{1}{2} I_o (1+\Delta_1)$$
$$I_2^{(1)} = \tfrac{1}{2} I_o (1-\Delta_1)$$

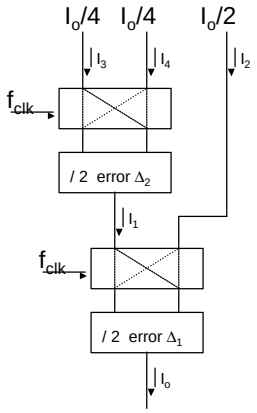
$$I_3^{(1)} = \tfrac{1}{2} I_1^{(1)} (1+\Delta_2)$$
$$= \tfrac{1}{4} I_o (1+\Delta_1)(1+\Delta_2)$$

During Φ_2

$$I_1^{(2)} = \tfrac{1}{2} I_o (1-\Delta_1)$$
$$I_2^{(2)} = \tfrac{1}{2} I_o (1+\Delta_1)$$

$$I_3^{(2)} = \tfrac{1}{2} I_1^{(2)} (1-\Delta_2)$$
$$= \tfrac{1}{4} I_o (1-\Delta_1)(1-\Delta_2)$$

$$\langle I_3 \rangle = \frac{I_3^{(1)} + I_3^{(2)}}{2}$$
$$= \frac{I_o}{4} \frac{(1+\Delta_1)(1+\Delta_2) + (1-\Delta_1)(1-\Delta_2)}{2}$$
$$= \frac{I_o}{4} (1+\Delta_1\Delta_2)$$



E.g. $\Delta_1 = \Delta_2 = 1\%$ → matching error is $(1\%)^2 = 0.01\%$