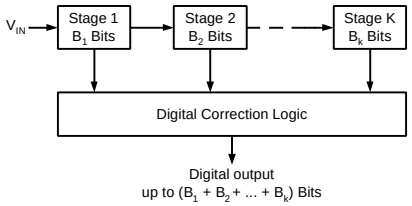
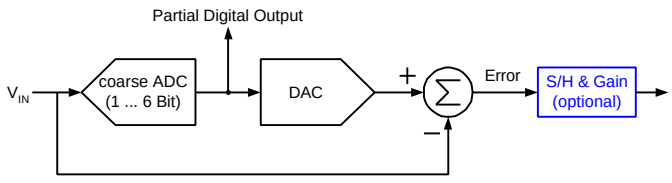
Pipelined A/D Converter

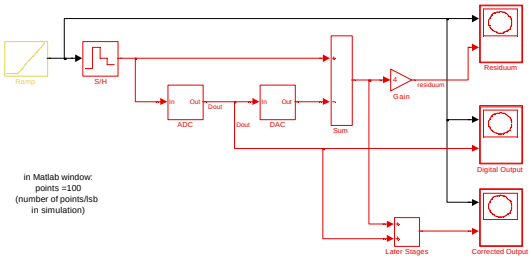
- Model
- Digital Correction
- Digital Calibration

Pipelined ADC





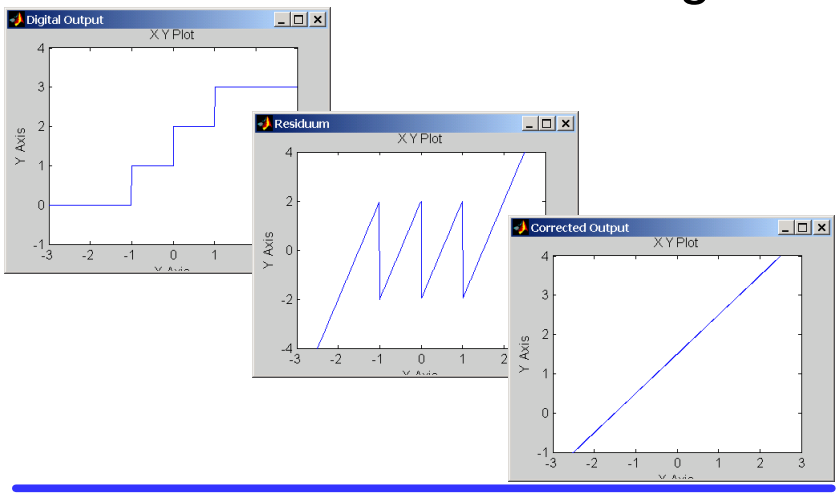
Pipeline Stage Model



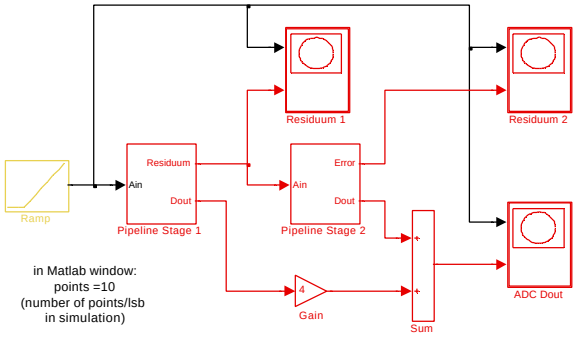
$$V_{res} = G\left(V_{in} - DV_{ref}\right)$$

See Matlab/Simulink L18_pipe_3_el.mdl

Simulation of 2-Bit Stage

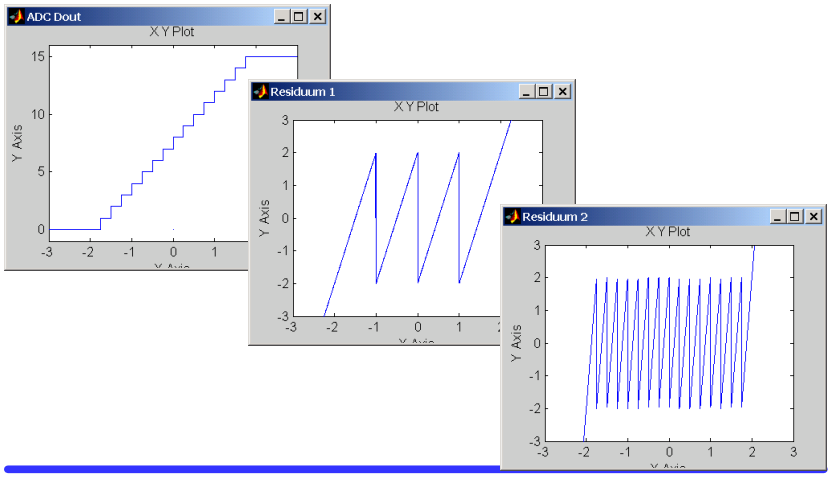


Pipeline ADC Model

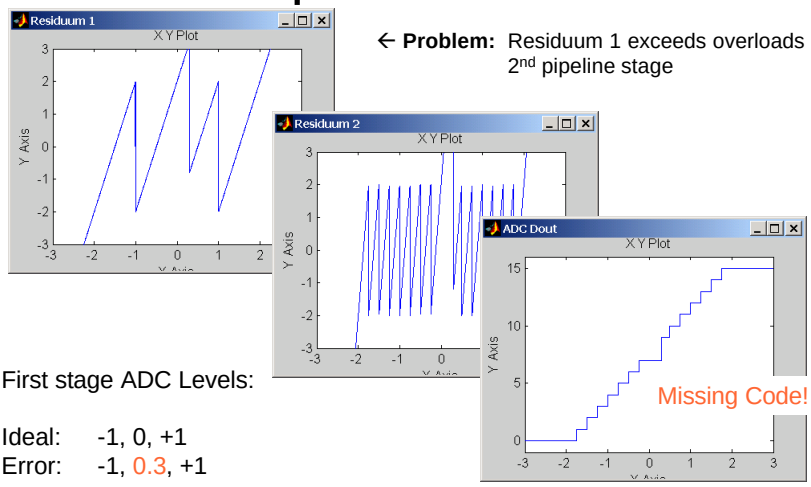


See Matlab/Simulink L18_pipe_2bps_error.mdl

Simulation Result



Comparator Offset



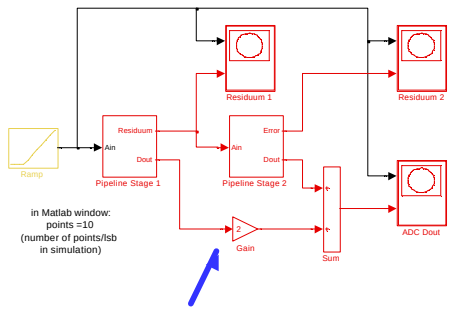
← **Problem:** Residuum 1 exceeds overloads 2nd pipeline stage

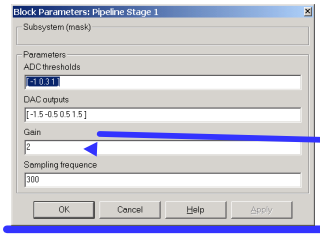
First stage ADC Levels:

Ideal: -1, 0, +1
Error: -1, 0.3, +1

Digital Correction

Pipeline ADC, 2 bits per stage
Interstage gain = 2 for digital correction

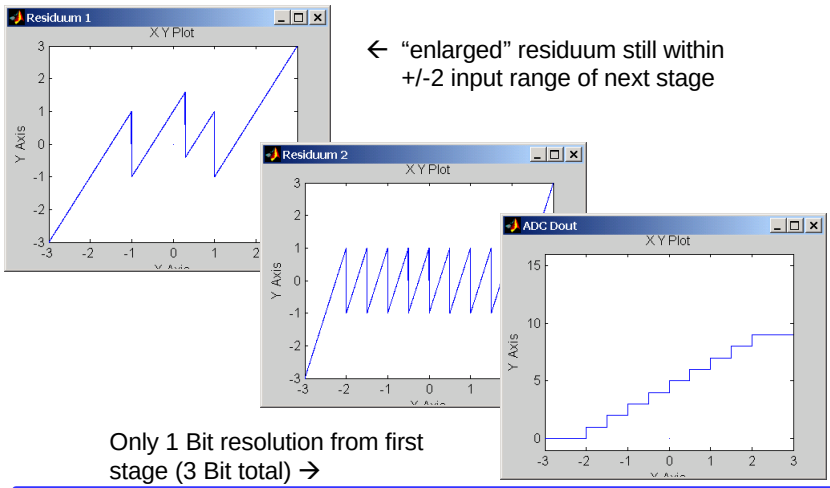




in Matlab window:
points =10
(number of points/lsb
in simulation)

Reduced interstage gain:
- No overload (due to comparator offset)
- Reduced input (only 1 bit resolution per stage)

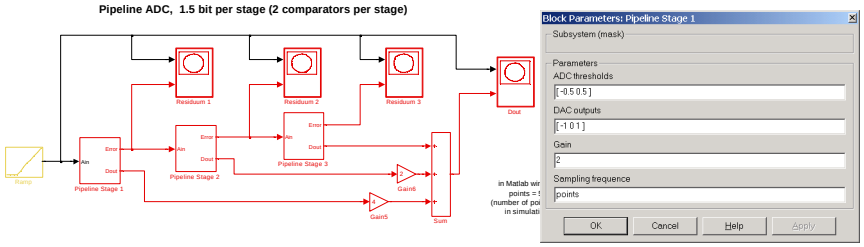
Digital Correction



← "enlarged" residuum still within +/-2 input range of next stage

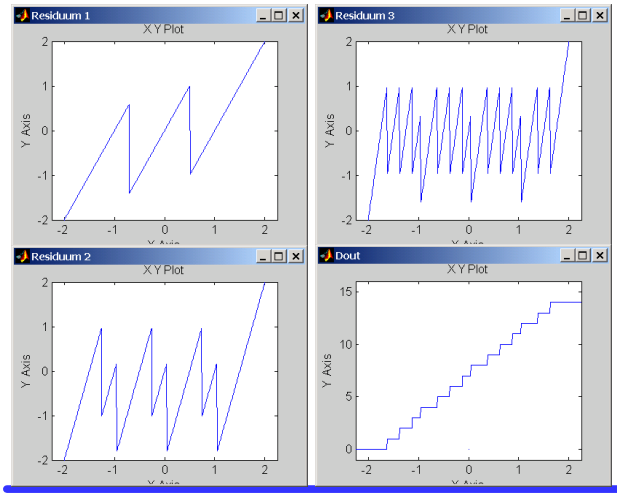
Only 1 Bit resolution from first stage (3 Bit total) →

"1.5-bps" Stage



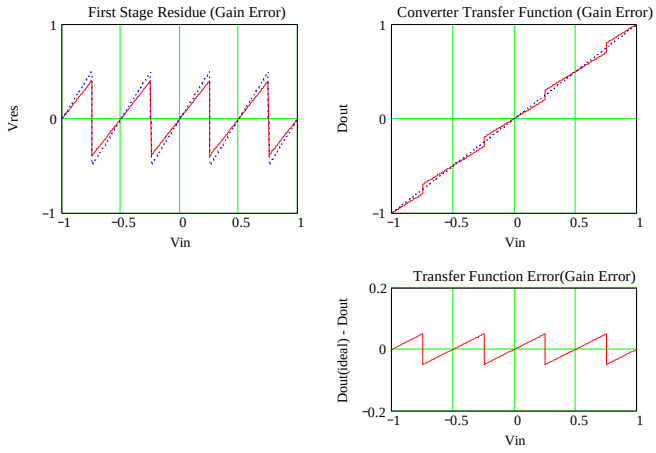
- A full bit of "overrange" is excessive for typical comparator offset
  - → use only 2 (rather than 3) comparators and G=2
- 3 DAC levels → lb(3) = 1.585 Bits
- Overall resolution:
  - 1 bps for all stages but last
  - 1.585 Bit for last

1.5-bps Pipeline



- What is the maximum offset that can be corrected?
- What is the offset of each comparator in this example?

Interstage Gain Error



Digital Gain Calibration

- Operation of the pipeline stage:

$$V_{res} = G\left(V_{in} - DV_{ref}\right)$$

The gain G is off from it's correct value (e.g. 1.8 instead of 2)

- Digital output from the ADC

$$GV_{in} = DGV_{ref} + V_{res}$$

  - Gain error (GV_{in} term)
  - Nonlinearity at segment boundary (DGV_{ref} term)

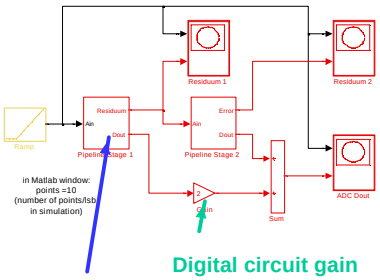
Digital Gain Calibration

$$GV_{in} = DGV_{ref} + V_{res}$$

- The "digital" gain in the circuit at right is still 2
- The actual amplifier gain in stage 1 is smaller or larger due to component mismatch
- E.g.

  GV_{ref} = 1000101101
  GV_{ref} = 1000000000

- Hence the overall output is incorrect, regardless of the accuracy of stage 2



Measuring GV_{ref}

- If we knew the value of GV_{ref}, we could use use that in our digital logic, rather than G=2
- How can we measure GV_{ref}?

$$V_{resA} = V_{res}(V_{in} = V_x, D = 0) = GV_x$$
$$V_{resB} = V_{res}(V_{in} = V_x, D = 1) = GV_x - GV_{ref}$$
$$V_{resA} - V_{resB} = GV_{ref}$$

- If we proceed from the back of the pipeline, we can use the already calibrated backend to digitize GV_{ref}!
- The measurement is performed once at startup, the values stored in a small RAM (one per stage for 1-bps stage resolution)
- The digital logic uses adders to sum up the different values of GV_{ref} from the table stored in the RAM

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A 15-b 1-Msample/s Digitally Self-Calibrated Pipeline ADC

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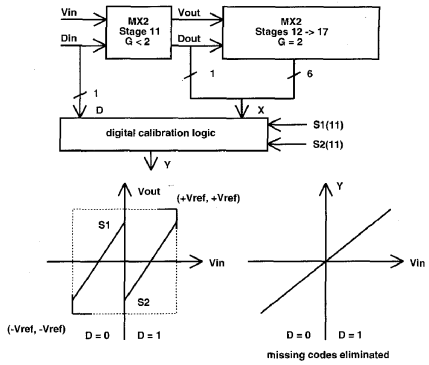

- 1-Bit per stage
- Only 1 comparator per stage
- G<2 to avoid overload in presence of comparator offset
- Digital gain calibration