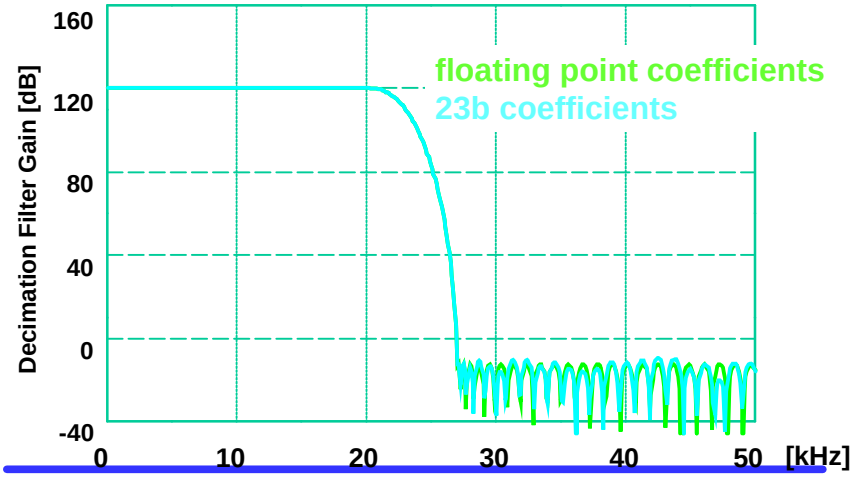
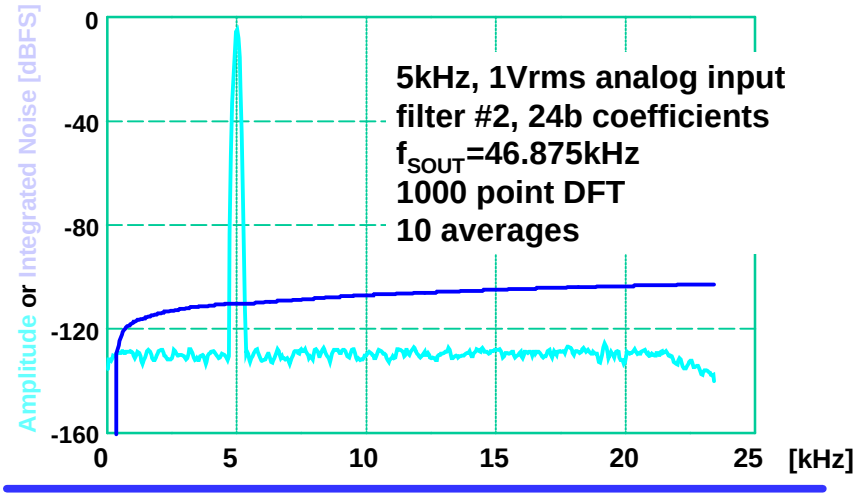
Today's Lecture

- Modeling the ΣΔ ADC decimation filter
  - Decimated DFTs
  - Fixed and floating point comparisons
  - Troubleshooting and test modes
- Multistage decimation filters
  - Parks-McClellan filters
  - Manual decimators
  - Hogenauer filters
  - Half-band filters

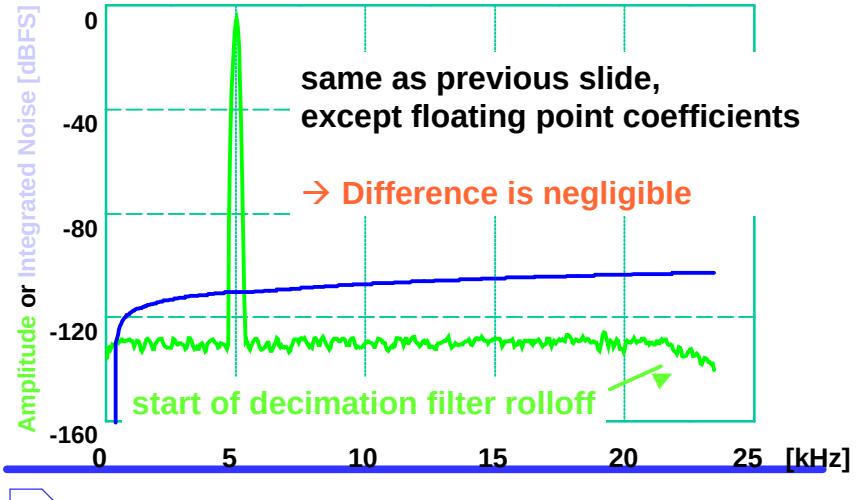
Filter #2 Responses



ΣΔ ADC Output DFT



ΣΔ ADC Output DFT



Production Testing

It's obvious that decimation filters obscure many details of modulator analog performance

- Most of the shaped quantization noise is filtered away
- Was the modulator fabricated correctly? Are there defects in a given chip?
- At this stage, you've got to consider possible production test modes…

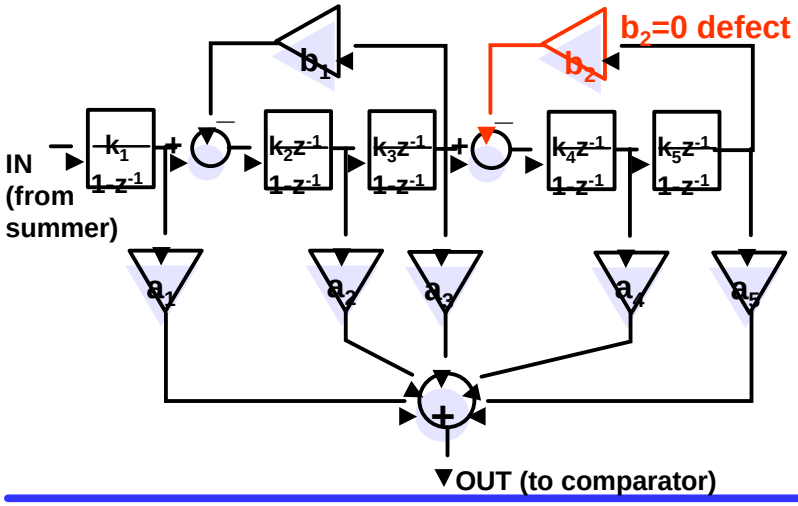
Test Modes

- All ΣΔ ADC designs must provide at least the following test modes:
  - Output unfiltered 1-bit modulator output samples
  - Insert test vectors at the decimation filter input
- Any mixed-signal IC which includes any ADC must provide for observability of unprocessed ADC output samples
  - Think of it as fault coverage in the analog domain
- Let's see how our decimation filter obscures a typical modulator manufacturing defect…

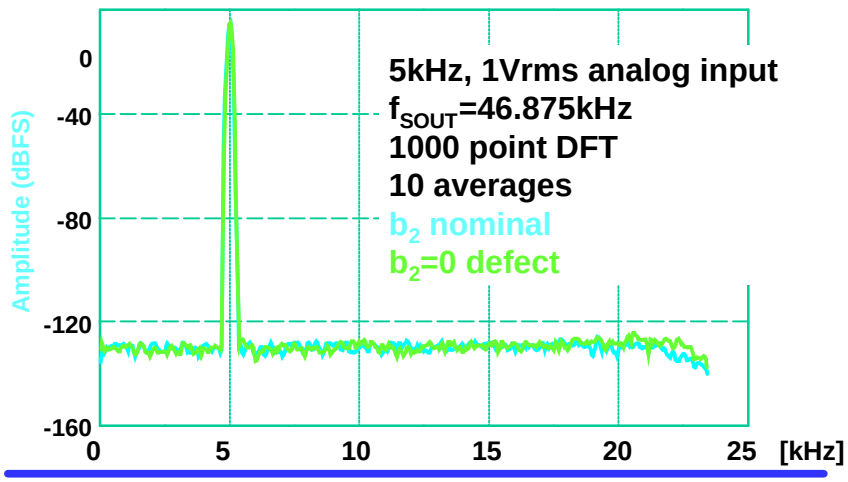
Test Modes

- Suppose the modulator is built with an open fault in a metal trace which connects up the switched capacitor implementing the b_2 capacitor
  - b_2 sets one of the quantization noise zeroes
  - If the b_2 capacitor is missing, b_2=0
  - In the real world, this defect will occur in 1-10ppm of production units
- The next two slides highlight the loop filter defect, and show decimated DFTs with and without the defect

Loop Filter Defect



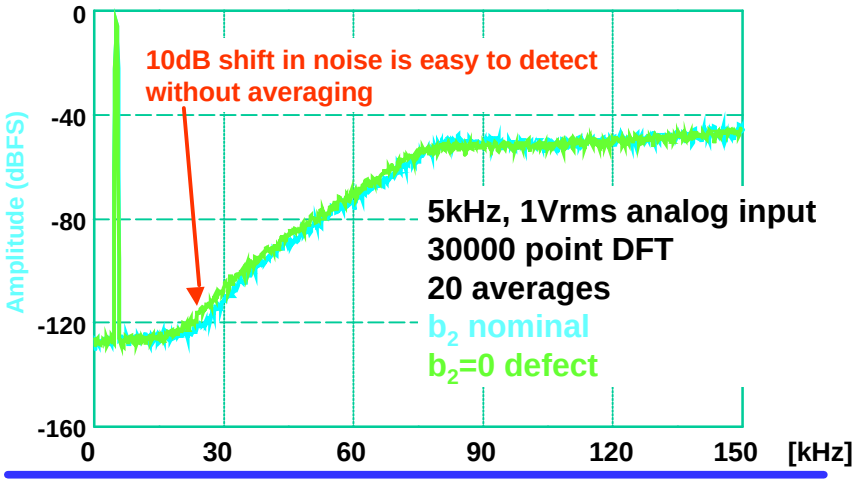
ΣΔ ADC Output DFT



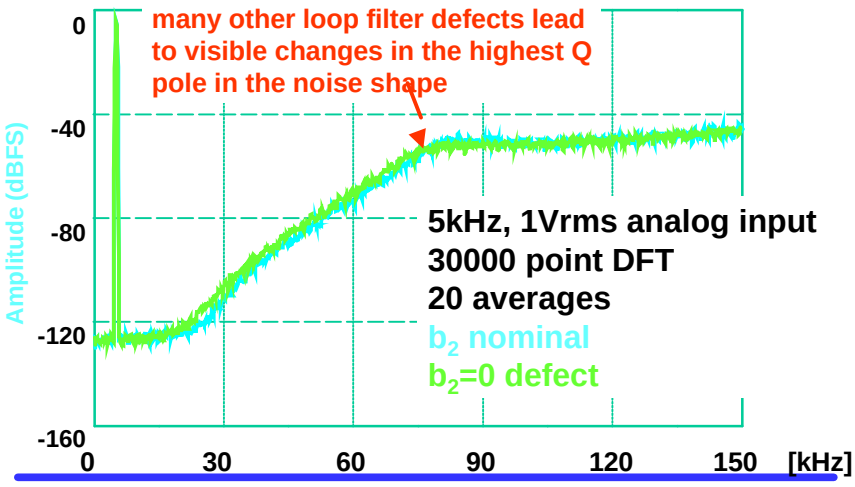
Test Modes

- The small increase in noise above 20kHz would probably be missed in production test
  - Dynamic range is specified to include only noise from 0-20kHz
- Should we ship the defective unit?
  - Absolutely not
  - The metal shrapnel pattern associated with the defect is unknown, and it may lead to a catastrophic failure later (reliability problem)
- Let's see if a 1-bit test mode can detect the fault …

ΣΔ ADC 1-bit Test Mode



ΣΔ ADC 1-bit Test Mode



Test Modes

- Models can analyze whether or not a specific defect is observable with a given test mode
  - Many defect-observability analyses are required to improve quality levels from ~100ppm defective to <10ppm defective
- These models improve over the production life of a chip and from generation-to-generation
  - If big customers detect a quality defect, they demand corrective action to improve tests so that units with the same defect won't be shipped again
  - Without 1-bit test modes, you're sunk!

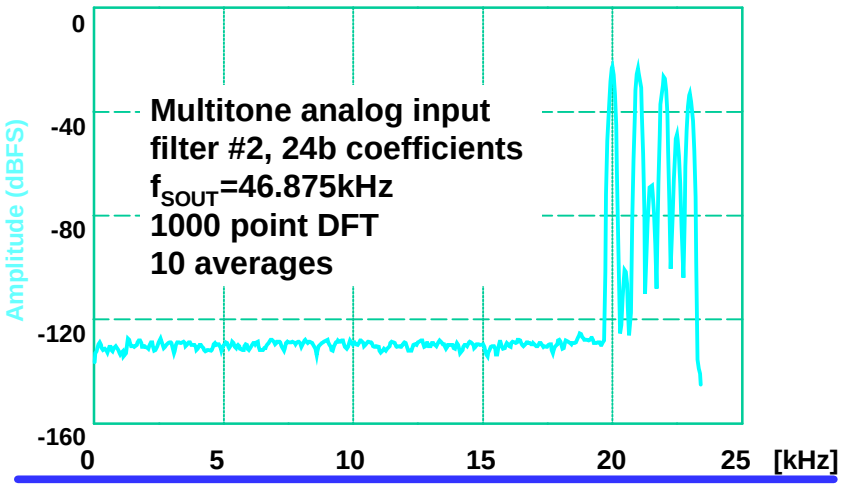
Multitone Tests

- As long as we're on the subject of testing, let's examine a fast, effective method to look at the frequency response of a filter or ADC
  - This method is used extensively in production tests of both analog filters and ADCs
  - It is <u>not</u> a substitute for classic, fault coverage testing of digital filters

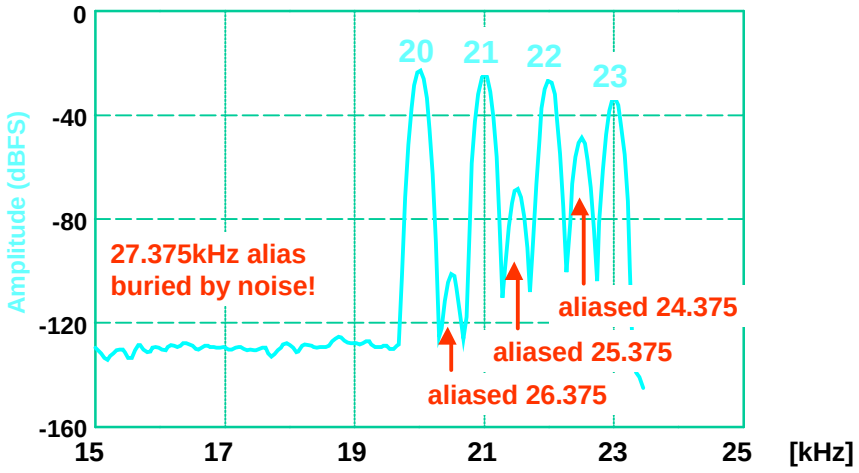
Multitone Tests

- IC testers can add sinewaves at many different frequencies in the digital domain
  - The digital sum is sent to a test system DAC which generates the analog input for a device under test
  - Frequency response at many different input frequencies can be determined with one test
- Let's see how our ΣΔ ADC responds to an input which is a sum of 20, 21, 22, 23, 24.375, 25.375, 26.375, and 27.375kHz sinewaves

ΣΔ ADC Multitone DFT



ΣΔ ADC Multitone DFT



Multitone Tests

- Note how elegantly the multitone output amplitudes trace the transition band of the decimation filter
- Total observation time (1000 ADC output samples) must be long enough to resolve each of the individual frequencies
  - Hz/bin is the reciprocal of the total observation time

Multistage Decimation Filters

- Decimation filter #2 can be realized with a accumulator rate of 57MHz, shift register, and coefficient ROM
  - Absolutely practical in today's CMOS processes
  - A multiplier is not needed
- Multi-rate decimators can achieve the same result with even lower processing cost
- We will:
  - Illustrate how multistage decimation requires substantially lower multiply-accumulate rates than single stage decimation
  - Introduce very specific filter architectures that are specialized just for decimation/interpolation and can further reduce hardware complexity

Multistage Decimation Filters

- In multistage decimation, implement the sharpest transition bands at the lowest sampling frequency
- For our 3MHz audio modulator, we'll decimate by 64 in 3 stages
  - 8X in the first stage
  - 4X in the second stage
  - 2X in the third stage

Multistage Decimation Filters

- Datapath precision is important here
  - Stage 1 has 1-bit input data and doesn't need a hardware multiplier
  - Intermediate rounding operations between stages 1 and 2 and between stages 2 and 3 add quantization noise which must be modeled in a "bit true" fashion
  - Final rounding to the 20-bit ADC output adds negligible noise
- Coefficient precision is also important
  - 24b precision for 135dB stopband attenuation

Parks-McClellan Decimation

- In the first pass with synthesize the three stages with the Parks-McClellan algorithm and stick with floating point numbers
  - The results provide an estimate of aggregate multiply accumulate rates
- Each stage will specify 0.0000±0.0033dB ripple from 0-20kHz
  - Passband ripple in the 3 stages may add
  - The goal is a "fair" comparison to filter #2

Parks-McClellan Decimation

- Stages 1 and 2 prevent decimation from aliasing noise and tones into frequencies below 27kHz
- Stage 1 stopbands:
  - 375±27kHz, 750±27kHz, 1125±27kHz, 1473-1500kHz
- Stage 2 stopbands:
  - 93.75±27kHz, 160.5-187.5kHz
- Stage 3 stopband: 27-46.875kHz
- For each stage we specify 135dB stopband attenuation

Parks-McClellan Decimation

- MATLAB's Parks-McClellan front end doesn't handle lowpass filters like stage 1 very easily
  - The low pass filter we want has a single passband, multiple stopbands, and interspersed don't care bands
- We'll waste zeroes and implement stages 1 and 2 as single-stopband LPFs:
  - Stage 1 stopband 348-1500kHz
  - Stage 2 stopband 66.75-187.5kHz
  - Stage 3 stopband still 27-46.875kHz

Parks-McClellan Decimation

- These Parks-McClellan designs yield:
  - Stage 1: Length 57 (21.375MHz)
  - Stage 2: Length 50 (4.688MHz)
  - Stage 3: Length 84 (3.938MHz)
- Multiply-accumulate rates are shown in red above
  - Total multiply-accumulate frequency is 30MHz
  - Exploiting linear phase coefficient symmetry can reduce this to 15MHz
  - The filter #2 design required 57MHz

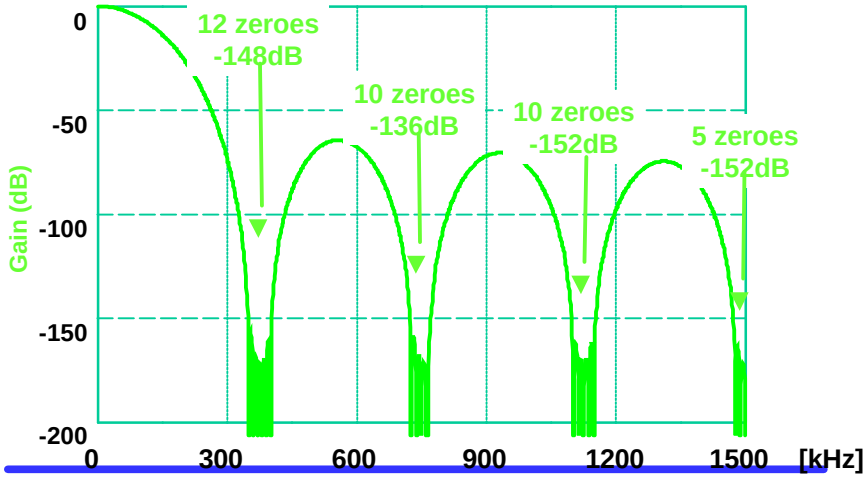
Parks-McClellan Decimation

- Stage 1 uses the most MAC cycles, but it doesn't need a hardware multiplier
- DSP conventional wisdom says you should always decimate (or interpolate) in stages
  - ΣΔ ADC decimation filters with 1-bit inputs are hardly conventional filters
  - Both single and multistage designs must be compared in power and area
- MACs required by unrelated DSP functions may have "free" cycles available for decimation

Manual Decimators

- Simple and effective first stage decimators spread unit circle zeroes evenly in areas where aliasing must be prevented
  - Start with about 5 zeroes per stopband
  - Add more if needed to reach –135dB in each band
- Our “manual decimator” requires only Length=38 to achieve specified performance
  - Zeroes at 350, 360, 370, 380, 390, 400, 726, 738, 750, 762, 764, 1101, 1113, 1125, 1137, 1149, 1476, 1488, and 1500kHz

Manual Decimator Response



Manual Decimators

- This decimator uses no zeroes off the unit circle, so its response droops (by 0.25dB) from dc to 20kHz
  - A Stage 3 Parks-McClellan filter can easily correct for this droop with little or no increase in order
- Manual zero placement reduces the Stage 1 MAC rate to 14.25MHz, a 33% reduction vs. the first-pass MATLAB solution (21.4MHz)

Clever Decimators

Two very clever decimation filter approaches which are occasionally very useful are

- Comb filters [1]
  - Implement (multiple) zeros on the unit circle very efficiently
- Half-band filters [2]
  - For very efficient 2X decimation/interpolation

Comb Filters

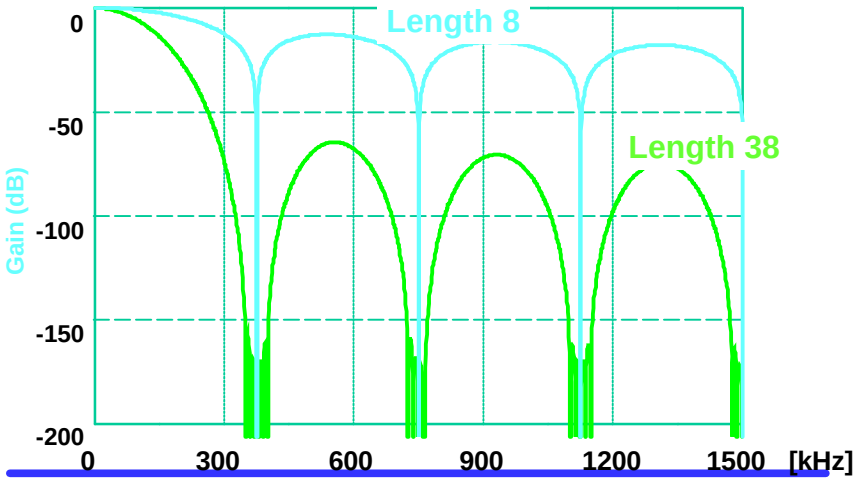
- Let's look at the a "rectangular" transfer function,

$$H(z) = \sum_{i=0}^{N-1} z^{-i}$$
$$= 1 + z^{-1} + z^{-2} + z^{-3} + z^{-4} + z^{-5} + z^{-6} + z^{-7} + \ldots$$
$$= \frac{1 - z^{-N}}{1 - z^{-1}}$$

- This filter has N-1 evenly spaced zeros on the unit circle, except at z=1 → LPF

- A N=8 rectangular window is the simplest filter candidate for a decimate-by-8 stage 1 design
  - Of course, its performance is unimpressive relative to our Length=38 manual decimator
  - At least the zeroes are in the right place …

Comb Decimator



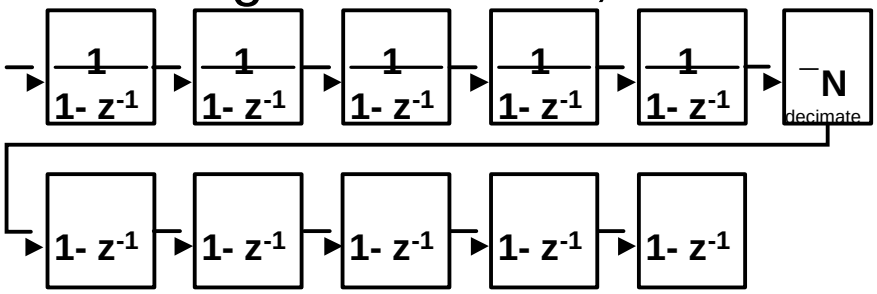
Comb Filters

- A single comb filter obviously will not meet the specification … but a cascade of K of them might
- The resulting filter is not very good (significant in-band droop), but a "trick" due to Hogenauer leads to an extraordinarily simple implementation

$$H(z) = \left[\sum_{i=0}^{N-1} z^{-i}\right]^K = \left[\frac{1-z^{-N}}{1-z^{-1}}\right]^K$$
$$= \left[\frac{1}{1-z^{-1}}\right]^K \left[1-z^{-N}\right]^K$$

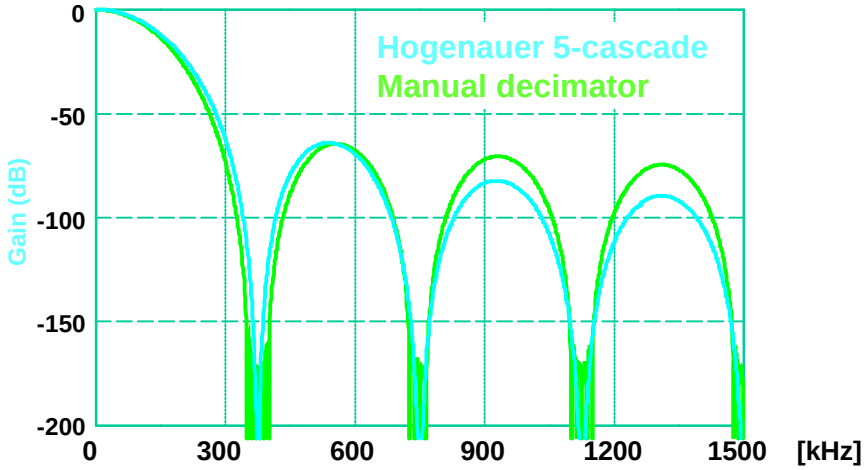
- Let's see how this looks in hardware …

Hogenauer Filter, K=5



- The integrators operate at f_{SIN}, the differentiators at f_{SOUT}
- The decimate block throws away N-1 of every N integrator output samples
- z^{-1} at f_{SOUT} is equivalent to z^{-N} at f_{SIN}

Hogenauer K=5 Cascade



Hogenauer Filters

- The Hogenauer 5-cascade doesn't come close to meeting our 135dB antialiasing specification near 375kHz
  - A higher value of K is needed (typically L+1 or more)
- Hogenauer implementations aren't without difficulty
  - The high-speed integrators integrate offsets to infinity and must "roll over" gracefully
  - Word-width requirements grow through the cascade
  - "Bit true" simulations are a must

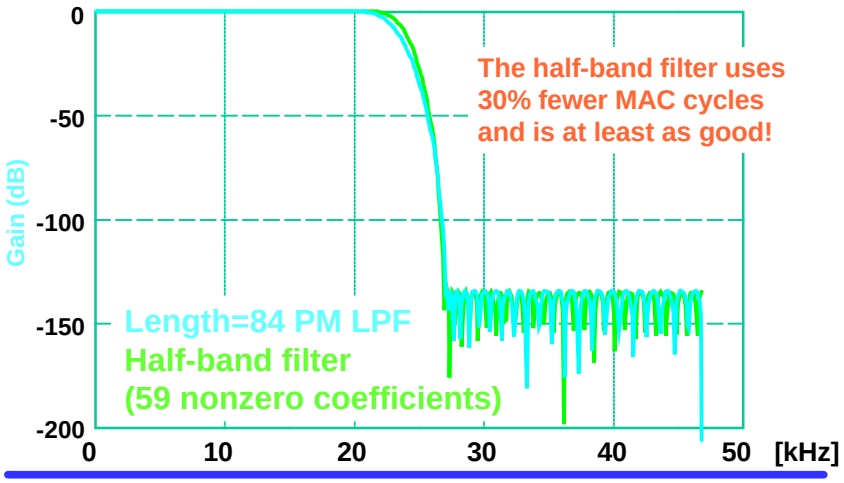
Half-band Filters

- Half-band filters [2] are very specialized linear phase low pass filters
  - They're useful only in decimate-by-2 (and interpolate-by-two) stages
  - They're useful only when some aliasing can be tolerated (-6dB gain at $f_{SOUT}/2$)
  - Half the coefficients (almost) are zero
    - Zero coefficients require no MAC cycles!
- Let's skip the derivation (see [2]) and look at an example …

Half-band Filters

- The response of a half-band stage 3 filter F(z) is symmetric (f_{SIN}=93.75kHz):
  - If F(z)'s gain is within $1\pm\varepsilon$ from 0-20kHz, its gain will be only ε from 26875-46875Hz
    - A good audio decimate-by-2 filter
  - The half-band filter inherently has –6dB gain at $f_s/4$ = 23437.5Hz
- But how can we get the Park-McClellan algorithm to design a half-band filter? The answer is in ref [2].
- Let's look at the response …

Half-band vs. PM Responses



References

[1] Eugene Hogenauer, “An Economical Class of Digital Filters for Decimation and Interpolation”, IEEE Trans. Acoustics, Speech, and Signal Processing, ASSP-29,April 1981.

[2] P. Vaidyanathn and T. Q. Nguyen, “A ‘Trick’ for the Design of FIR Half-band Filters”, IEEE Trans. Circuits Sys., CAS-34, pp. 297-300, March 1987.